# Synchronous Step-Down DC/DC Controller

## General Description

The AS2318 is a Buck controller designed for USB power delivery (USB-PD). It operates with wide input voltage range from 4.5V to 36V, and the output voltage is adjustment from 3V to 28V. The AS2318 implements current mode control mechanism with the constant voltage (CV) and constant current (CC) output to support USB-PD. The AS2318 fault protection includes cycle-by-cycle current limit, short circuit protection, UVLO and thermal shutdown. The soft-start function prevents inrush current at turn-on. This device uses current mode control scheme which provides fast transient response. Internal compensation function reduces external compensatory components and simplifies the design process. In shutdown mode, the supply current is about 20μA.

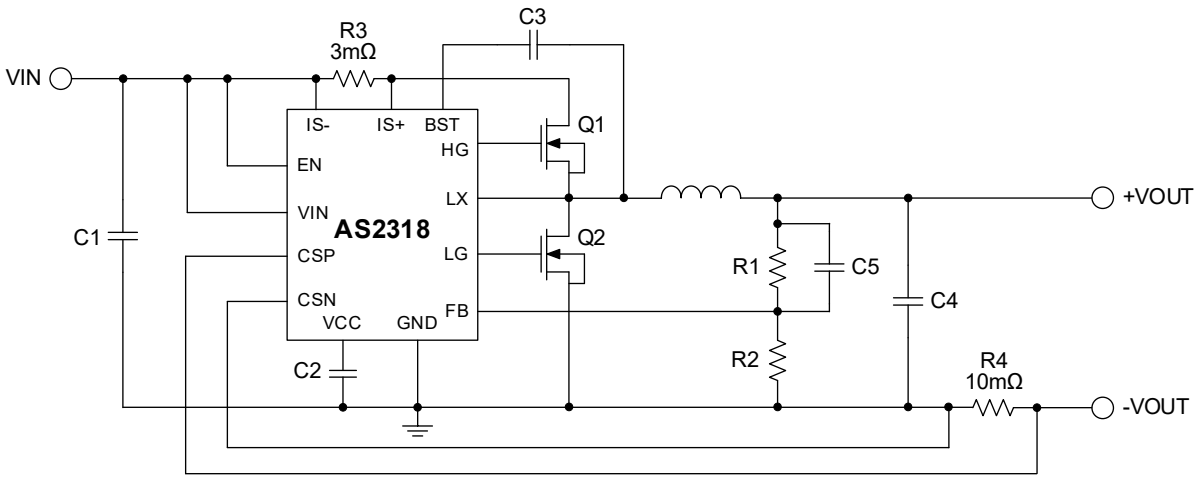
## Features

- Wide Input Voltage Range: 4.5V to 36V
- Adjustable Output Voltage Range: 3V to 28V
- 5A Output Current
- 130kHz Switching Frequency
- Supports CC/CV Mode Control
- 1mA Quiescent Current
- Internal 3ms Soft-Start
- Internal Compensation Function
- Cycle-by-Cycle Current Limit
- Hiccup Short Circuit Protection
- Input Under Voltage Lockout
- Input Over Voltage Protection
- Cable Voltage Drop Compensation
- Over-Temperature Protection with Auto Recovery
- TDFN-12L (3mm x 3mm) Package

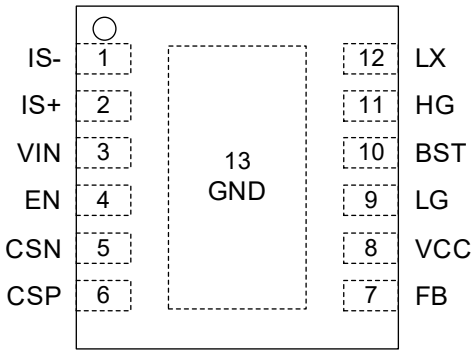
## Application

- Car Charger
- Portable Charger Application
- Smart Power Strip

## Typical Application Circuit



## Pin Configuration




TDFN-12L

## Pin Descriptions

| Pin | Name | Function |
|---|---|---|
| 1 | IS- | Current sense negative input pin. |
| 2 | IS+ | Current sense positive input pin. |
| 3 | VIN | Power supply input pin. |
| 4 | EN | Enable logic input. Logic high level enables the device and logic low level disables the device. |
| 5 | CSN | current sense (-) input pin. |
| 6 | CSP | current sense (+) input pin. |
| 7 | FB | Voltage feedback input pin. Connect FB and VOUT with a resistive voltage divider. This IC senses feedback voltage via FB and regulates it at 0.8V. |
| 8 | VCC | Internal regulator output. Connect a 1uF capacitor to GND to stabilize the internal regulator voltage. |
| 9 | LG | Low side gate drive |
| 10 | BST | High side gate drive boost pin. A capacitance 100nF must be connected from this pin to LX. It can boost the gate drive to fully turn on the internal high side NMOS. |
| 11 | HG | High side gate drive |
| 12 | LX | Power switching node. |
| 13 | Exposed Pad | Connect the exposed pad to GND. |

## Ordering Information

| PART No. | PACKAGE | Logo | Tape & Reel |
|---|---|---|---|
| AS2318 | TDFN-12L | AS2318 | 3000PCS |

## Absolute Maximum Ratings (1)

| Parameter | Value | Unit |
|---|---|---|
| Supply Voltage $V_{IN}$ | -0.3 to 40 | V |
| Enable Voltage $V_{EN}$ | -0.3 to 40 | V |
| LX Voltage $V_{LX}$ | -0.3 to $V_{IN}$ + 0.3 | V |
| BST Pin Voltage $V_{BST}$ | -0.3 to $V_{LX}$ + 7 | V |
| All Other Pins Voltage | -0.3 to 6 | V |
| Maximum Junction Temperature ($T_J$) | 150 | °C |
| Storage Temperature ($T_S$) | -65 to 150 | °C |
| Lead Temperature (Soldering, 10sec.) | 260 | °C |
| Package Thermal Resistance, ($\theta_{JA}$) (2) | TBD | |
| Package Thermal Resistance, ($\theta_{JC}$) (2) | TBD | |

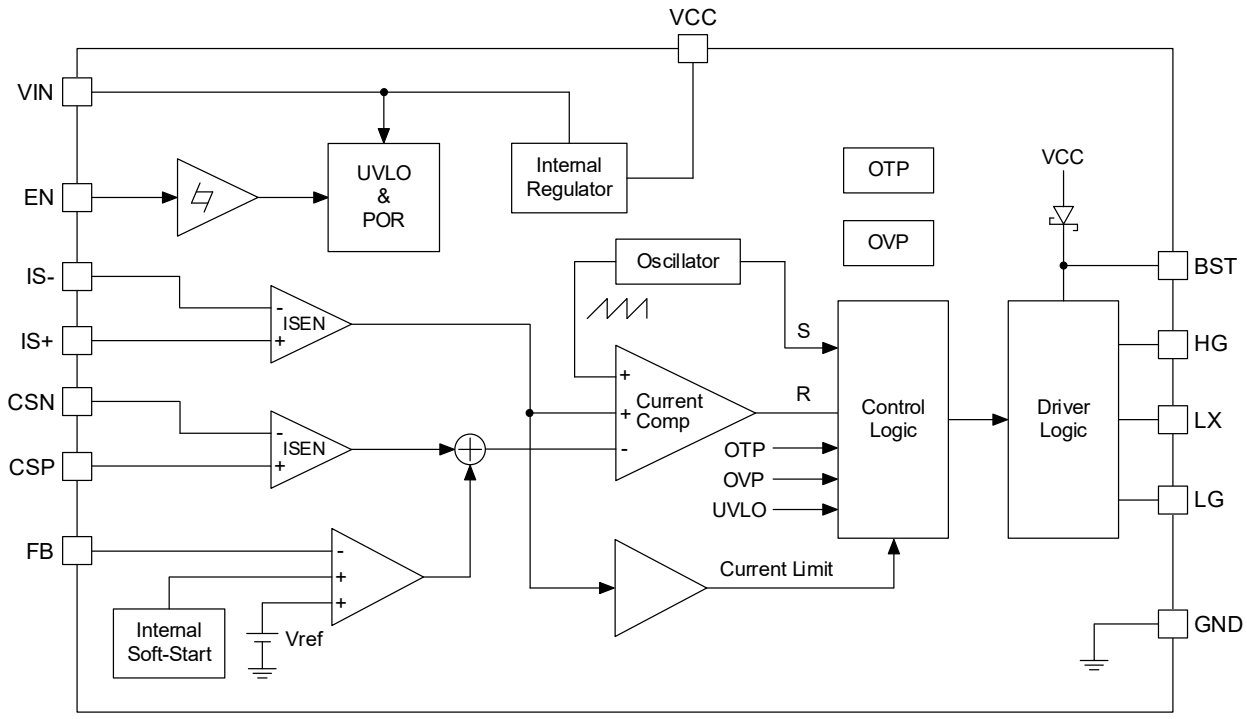
**NOTE:**

1. Stresses beyond this listed under "*Absolute Maximum Ratings*" may cause permanent damage to the device.
2. $\theta_{JA}$ is measured at 25°C ambient with the component mounted on a high effective thermal conductivity 4-layer board of JEDEC-51-7. $\theta_{JC}$ is measured on the exposed pad. The thermal resistance greatly varies with layout, copper thickness, number of layers and PCB size.

## Recommended Operating Conditions

| Parameter | Value | Unit |
|---|---|---|
| Supply Voltage $V_{IN}$ | 4.5 to 36 | V |
| Operation Temperature Range | -40 to 85 | °C |
| Operation Junction Temperature Range | -40 to 125 | °C |

## Block Diagram



# Electrical Characteristics

($V_{IN}$ = 12V, $T_A$ = 25°C, unless otherwise noted.)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | $V_{IN}$ Input Supply Voltage | | 4.5 | | 36 | V |
| $V_{IN\_OVP}$ | Input Over Voltage Protection | | | 37.5 | | V |
| $V_{UVLO(on)}$ | $V_{IN}$ Under voltage Lockout Threshold | $V_{IN}$ Rising | | 4.15 | | V |
| $V_{UVLO(HYS)}$ | Under Voltage Lockout Threshold Hysteresis | EN = GND | | 250 | | mV |
| $I_{SD}$ | $V_{IN}$ Shutdown Current | | | 20 | | μA |
| $I_{DDQ}$ | $V_{IN}$ Quiescent Current | $V_{FB}$ = 1V | | 0.7 | | mA |
| $V_{FB}$ | Feedback Voltage | 4.5V ≤ $V_{IN}$ ≤ 36V | 0.788 | 0.8 | 0.812 | V |
| $T_{SS}$ | Internal Soft-Start Time | | | 3 | | ms |
| $F_{OSC}$ | Oscillation Frequency | $V_{IN}$ = 12V | 110 | 130 | 150 | kHz |
| $D_{MAX}$ | Maximum Duty Cycle | | | 98 | | % |
| $T_{ON}$ | Minimum On Time (1) | | | 150 | | ns |
| $T_{OFF}$ | Minimum Off Time (1) | | | 192 | | ns |
| $R_{HS\_UP}$ | High side driver pull up resistor | | | 10 | | Ω |
| $R_{HS\_DOWN}$ | High side driver pull down resistor | | | 2 | | Ω |
| $R_{LS\_UP}$ | Low side driver pull up resistor | | | 5 | | Ω |
| $R_{LS\_DOWN}$ | Low side driver pull down resistor | | | 1.5 | | Ω |
| DT1 | Dead time for HS off to LS on | | | 25 | | ns |
| DT2 | Dead time for LS off to HS on | | | 25 | | ns |
| $V_{EN}$ | EN Input Low Voltage | | | | 2.2 | V |
| $V_{EN}$ | EN Input High Voltage | | 2.7 | | | V |
| $I_{EN}$ | EN Current | $V_{EN}$ = 2V | | 2 | | μA |
| $T_{SS}$ | Internal Soft-Start Period | | | 3 | | ms |
| $I_{LIM}$ | High Side Current Limit | R3 = 3mΩ | | 10 | | A |
| $V_{CS}$ | CS Sense Voltage | R4 = 10mΩ | 33.5 | 36 | 38.5 | mV |
| | Cable Compensation | R4 = 10mΩ | 90 | 100 | 110 | mV/A |
| $T_{SD}$ | Thermal Shutdown Threshold (1) | | | 150 | | °C |
| $T_{SD(HYS)}$ | Thermal Shutdown Hysteresis (1) | | | 50 | | °C |

**NOTE:**

1. Not production tested.

# Functional Description

The AS2318 is a Buck controller designed for USB power delivery (USB-PD), and provides 5A continuous load current. It regulates input voltage from 4.5V to 36V and down to an output voltage as low as 0.8V.

## Internal Compensation Function

The stability of the feedback circuit is controlled by internal compensation circuits. This internal compensation function is optimized for most applications, and this function can reduce external R, C components.

## Soft Start

The AS2318 employs internal soft start function to reduce input inrush current during start up. The typical value of internal soft start time is 3ms.

## Input Under Voltage Lockout

When the AS2318 is power on, the internal circuits will be held inactive until $V_{IN}$ voltage exceeds the input UVLO threshold voltage. And the regulator will be disabled when $V_{IN}$ is below the input UVLO threshold voltage. The hysteretic of the UVLO comparator is 250mV (typ).

## Constant Voltage / Constant Current Mode

AS2318 operates either in CV (constant voltage) mode or CC (constant current) mode and automatically changes from CV to CC smoothly. In CV mode, AS2318 regulates the output voltage. As long as output current limit threshold is reached, AS2318 enters CC mode and the output voltage drops while output current is clamped at the setting values.

## Cable Voltage Drop Compensation

The AS2318 is capable of compensating the output voltage drop, caused by a long trace, to keep a fairly constant 5V load-side voltage. When using default 10mΩ output sensing resistor, the AS2318 provides 100mV/A fixed line drop compensation rate for long cables.

## Over Current Protection

The AS2318 over current protection function is implemented by using cycle-by-cycle current limit architecture. The inductor current is monitored by measuring the high-side MOSFET series sense resistor voltage. When the load current increases, the inductor current will also increase. When the peak inductor current reaches the current limit threshold, the output voltage will start to drop. When the over current condition is removed, the output voltage will return to the regulated value. The peak current of inductor can be set by external $I_{LIM}$ resistor (R3) by the following equation.

$$I_{LIM} = \frac{30mV}{R3}$$

## Short Circuit Protection

The AS2318 provides short circuit protection function to prevent the device damaged from short condition. When the short condition occurs and the feedback voltage drops lower than 0.3V, hiccup mode will be triggered to prevent the AS2318 from overheating during the extended short condition. Once the short condition is removed, the AS2318 will end the hiccup mode and return to normal.

### Over Temperature Protection

The AS2318 incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown. And the hysteretic of the over temperature protection is 50°C (typ).

### Input Over Voltage Protection

The AS2318 supports input over voltage protection. When input voltage exceeds the input over Voltage threshold, the regulator will be shutdown unless the input over voltage is removed. The hysteretic of the input OVP comparator is 2V (typ).

## Applications Information

### Output Voltage Setting

The output voltage $V_{OUT}$ is set using a resistive divider from the output to FB. The FB pin regulated voltage is 0.8V. Thus the output voltage equation is:

$$V_{OUT} = 0.8V \times \left(1 + \frac{R1}{R2}\right)$$

### CC Current Setting

AS2318 constant current value is set by the resistor R4 connected between the CS and GND pins. In the CC mode, the voltage of CS pin will be regulated to 36mV. The CC current value is calculated as:

$$I_{CS} = \frac{36mV}{R4}$$

### Input Capacitor Selection

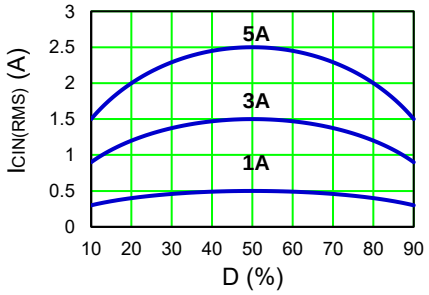
The use of the input capacitor is filtering the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

Where D is the duty cycle of the power MOSFET.

This function reaches the maximum value at D=0.5 and the equivalent RMS current is equal to $I_{OUT}/2$. The following diagram is the graphical representation of above equation.



A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice. When using tantalum or electrolytic capacitors, a 0.1μF ceramic capacitor should be placed as close to the IC as possible.

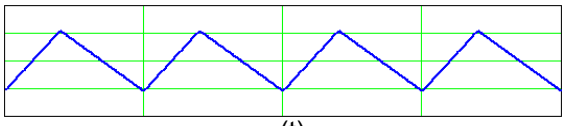
## Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. When operating in constant current mode, the output ripple is determined by four components:

$$V_{RIPPLE}(t) = V_{RIPPLE(C)}(t) + V_{RIPPLE(ESR)}(t) + V_{RIPPLR(ESL)}(t) + V_{NOISE}(t)$$

The following figures show the form of the ripple contributions.

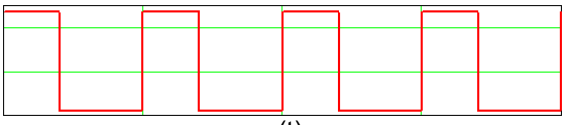
$V_{RIPPLE(ESR)}$ (t)



(t)

+

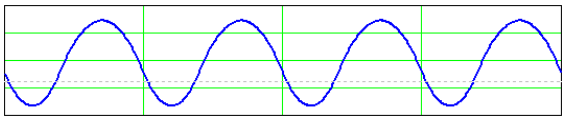
$V_{RIPPLE(ESL)}$ (t)



(t)

+

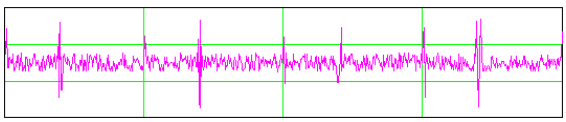
$V_{RIPPLE(C)}$ (t)



(t)

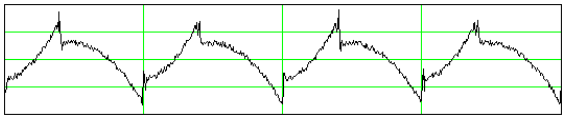
+

$V_{NOISE}$ (t)



=

$V_{RIPPLE}$ (t)



(t)

$$V_{RIPPLE(ESR)} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times ESR$$

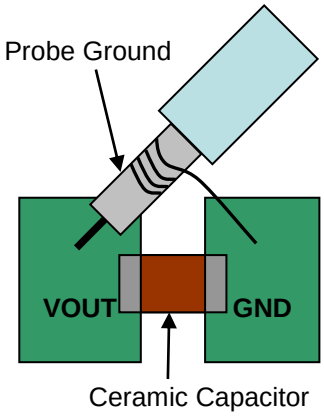
$$V_{RIPPLE(ESL)} = \frac{ESL}{L} \times V_{IN}$$

$$V_{RIPPLE(C)} = \frac{V_{OUT}}{8 \times F_{OSC^2} \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where $F_{OSC}$ is the switching frequency, L is the inductance value, $V_{IN}$ is the input voltage, ESR is the equivalent series resistance value of the output capacitor, ESL is the equivalent series inductance value of the output capacitor and the $C_{OUT}$ is the output capacitor.

Low ESR capacitors are preferred to use. Ceramic, tantalum or low ESR electrolytic capacitors can be used depending on the output ripple requirement. When using the ceramic capacitors, the ESL component is usually negligible.

It is important to use the proper method to eliminate high frequency noise when measuring the output ripple. The figure shows how to locate the probe across the capacitor when measuring output ripple. Removing the scope probe plastic jacket in order to expose the ground at the tip of the probe. It gives a very short connection from the probe ground to the capacitor and eliminating noise.



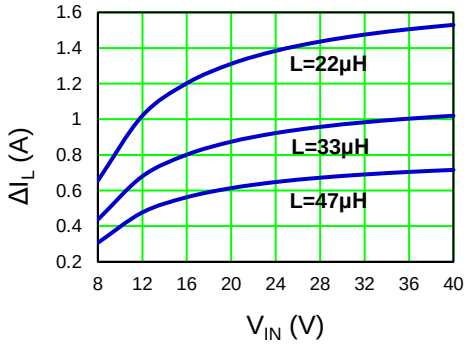

## Inductor Selection

The output inductor is used for storing energy and filtering output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode.

That will lower ripple current and result in lower output ripple voltage. The $\Delta I_L$ is inductor peak-to-peak ripple current:

$$\Delta I_L = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The following diagram is an example to graphically represent $\Delta I_L$ equation.




$V_{OUT}$=5V, $F_{OSC}$=130kHz

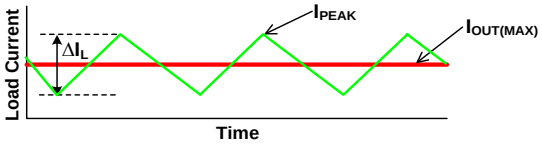
A good compromise value between size and efficiency is to set the peak-to-peak inductor ripple current $\Delta I_L$ equal to 30% of the maximum load current. But setting the peak-to-peak inductor ripple current $\Delta I_L$ between 20%~50% of the maximum load current is also acceptable. Then the inductance can be calculated with the following equation:

$$\Delta I_L = 0.3 \times I_{OUT(MAX)}$$

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{OSC} \times \Delta I_L}$$

To guarantee sufficient output current, peak inductor current must be lower than the AS2318 high-side MOSFET current limit. The peak inductor current is shown as below:

$$I_{PEAK} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$



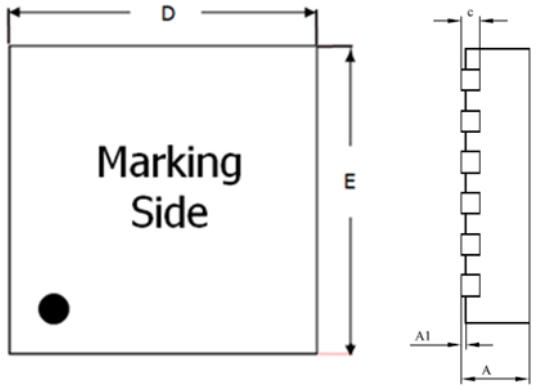

## PCB Layout Recommendations

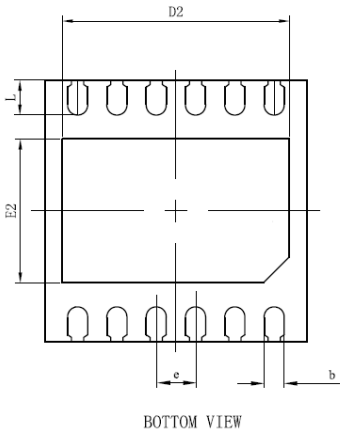
The proper PCB layout and component placement are critical for all switch mode power supplies. The noise-sensitive feedback and compensation circuitry are isolated from the high-frequency switching nodes. The careful attention should be taken to the high-frequency and high current loops. Use wide and short traces for the main current paths. Here are some suggestions to the layout of AS2318 design.

1. Place the input capacitors and output capacitors as close to the device as possible. Trace to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (LX).
4. The exposed pad of the package should be soldered to an equal amount of metal area on the PCB.
5. The VIN and LX plane area connecting to the exposed pad should be maximized, and use multiple vias to connect to the intermediate PCB power plane.
6. The GND plane area and connecting vias should be maximized to improve thermal performance.
7. Multi-layer PCB design is recommended.

# Package Information

## TDFN-12L




| SYMBOLS UNIT | DIMENSION IN MILLIMETER | |
|---|---|---|
| | MIN | MAX |
| A | 0.70 | 0.90 |
| A1 | 0.00 | 0.05 |
| C | 0.203REF | |
| E | 2.90 | 3.10 |
| D | 2.90 | 3.10 |
| L | 0.30 | 0.50 |
| b | 0.15 | 0.30 |
| e | 0.450 BSC | |
| D2 | 2.20 | 2.60 |
| E2 | 1.35 | 1.65 |