Critical Conduction Mode PFC Controller

General Description

The AS2562 family are critical conduction mode (CrM) power factor correction (PFC) controller for high performance AC/DC power system. With the highly linear multiplier and THD optimizer, the AS2562 can achieve ultra-low THD and near unity power factor under different operation conditions. The AS2562 operates over a wide supply voltage range from 11V to 30V, which is suitable for a variety of application scenarios. Ultra-low startup current and optimized VCC undervoltage protection make startup easier for self-powered systems. In application scenarios that focus on light-load efficiency, AS2562 can choose to enter the discontinuous conduction mode (DCM). In this mode, when the switching frequency exceeds the frequency clamping threshold, the circuit operates in DCM with valley turn-on. The Intelligent protection functions and strategies of AS2562 can effectively reduce MOSFET electrical stress and greatly improve system reliability, such as soft-start and soft-stop protection, brown in brown out protection, smart high/low line overcurrent protection, etc.

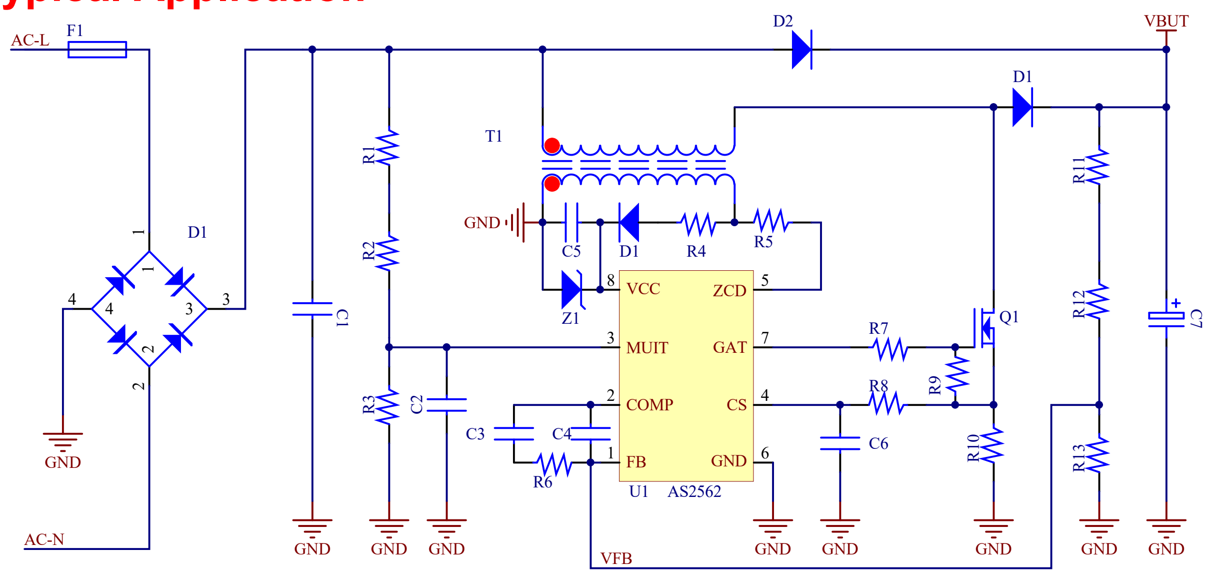
Features

- Operates in a Wide VCC Voltage Range from 11V-30V
- Ultra-Low Quiescent Current: <160uA
- Ultra-Low Startup Current: <20uA
- Total Harmonic Compensator for AC Zero-Crossing
- Ultra-low THD & Unity Power Factor
- Smart High/Low Line Overcurrent Protection
- Maximum Operating Frequency Limit and Valley Switching
- On-Chip Current Sense Filter
- Brown-In Brown-Out Protection
- Noise Immunity Enhancement
- Feedback Open Loop Protection
- Gate Driving Capability: +/- 0.8A
- Package: SOP-8

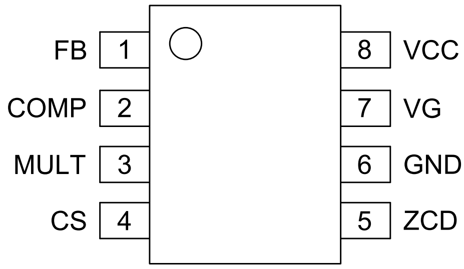
Applications

- AC/DC Adapters/Charger
- Industrial Power Supplies
- TV, Desktop PC, Monitor
- Lighting Application

Typical Application



Pin Configuration



SOP-8

Pin Descriptions

Pin	Name	Description
1	FB	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and FB (pin#1) to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine MOSFET's turn-off.
5	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
6	GND	Ground. Current return for both the signal part of the IC and the gate driver.
7	VG	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 800 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12V to avoid excessive gate voltages in case VCC is supplied with a higher voltage level.
8	VCC	Supply Voltage of both the signal part of the IC and the gate driver.

Absolute Maximum Ratings [1]

Symbol	Parameter	MIN	MAX	Units
VCC	supply voltage VCC	-0.3	32	V
FB, COMP, MULT, CS[2]	voltage on pin FB, COMP, MULT, CS	-0.3	8	
VG [2]	voltage on pin VG	-0.3	14	
I_{ZCD}	ZCD max current	-1	1	mA
T_J	operating junction temperature,	-40	150	°C
T_{stg}	storage temperature	-55	150	
T_{sld}	soldering temperature (10 second)		260	

Notes:

(1) Stresses beyond the “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in “RECOMMENED OPERATING CONDITIONS”. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Output pin not to be voltage driven.

Recommended Operating Conditions

		MIN	MAX	Units
Recommended Operation Conditions	VCC supply voltage	11	30	V
	operating junction temperature. (T_J)	-40	125	°C

Thermal Information

		Value	Units
Package Thermal Resistance [1]	θ_{JA} (Junction to ambient)	128	°C/W
	θ_{JC} (Junction to case)	75	

Note：

(1) Measured on JESD51-7, 4-layer PCB.

Electrical Characteristics

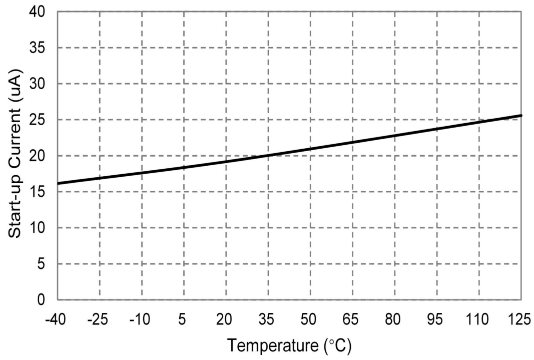
-40°C ≤ $T_A = T_J$ ≤ 125°C. V_{CC} = 13V_{DC}, 1μF from VCC to GND. All voltages are measured with respect to ground (pin 6). Currents are positive when flowing into the IC, unless otherwise specified.

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
Supply Current						
I_{st}	Start-up current	Before turn-on, V_{CC}=11V		20	35	μA
I_q	Quiescent current	V_{CC}=13V, FB=3V		160	230	μA
I_{op}	Operating supply current	F_{sw}=70kHz, C_{load}=1nF at VG		1.3	2.5	mA
Supply Voltage						
V_{CC}	Operating range	After turn-on	11		30	V
V_{CC_ON}	Turn-on threshold		11	12	13	V
V_{CC_OFF}	Turn-off threshold		8.7	9.5	10.5	V
V_{CC_Hys}	Threshold hysteresis		2		3	V
V_Z	VCC holding threshold	I_{CC}=20mA	30	32	35	V
Multiplier Input						
I_{mult}	Input bias current	Vmult=2V			1	μA
V_{mult}	Linear operating range		0 to 3			V
$\Delta V_{CS}/\Delta V_{mult}$	Output max slope	Vcomp=upper clamp, Vmult=0V to 0.5V		2		V/V
K	Multiplier output gain	Vmult=1V, Vcomp=4V		0.6		1/V
Error Amplifier						
V_{FB}	Feedback voltage threshold	10V<VCC<30V		2.5		V
I_{FB}	Input bias current	Vfb=2.5V			1	μA
I_{COMP}	Source current	V_{COMP}=4V, V_{FB}=2.4V		3.6		mA
	Sink current	V_{COMP}=4V, V_{FB}=2.6V		5.7		mA
V_{COMP}	Upper clamp voltage	I_{source}=0.5mA, VCC=13V	5.4	5.9	6.5	V
	Lower clamp voltage	I_{sink}=0.1mA, VCC=13V	2	2.15	2.3	V
Brown-In Brown-Out Protection and Line Feed Forward						
V_{BI}	Brown-in Threshold		0.8	0.9	1	V
V_{BO}	Brown-out Threshold		0.7	0.8	0.9	V
V_{HL}	Comparator threshold for high line detection		1.9	2	2.1	V
V_{LL}	Comparator threshold for low line detection		1.6	1.7	1.8	V

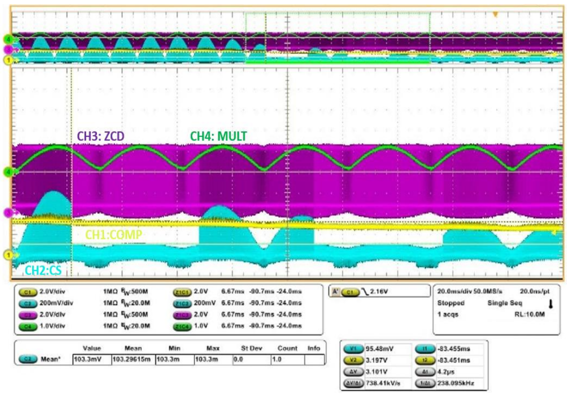
Output Overvoltage						
I_{OVP}	Dynamic OVP triggering current		20	33	45	μA
I_{OVP_Hys}	Dynamic OVP current hysteresis(1)			20		μA
V_{OVP}	Static OVP threshold		2	2.15	2.3	V
Current Sense Comparator						
I_{CS}	Input bias current	V_{CS}=1V			1	μA
T_{dly}	Delay to output(1)			100		ns
V_{CS_offset}	Current sense offset(1)	V_{mult}=0V		30		mV
		V_{mult}=3V		0		
V_{CS_OC}	OC threshold	Vcomp=upper clamp	1.6	1.7	1.8	V
$V_{CS\_OC\_LL}$	OC threshold when low line is detected	Vcomp=upper clamp	1.6	1.7	1.8	V
$V_{CS\_OC\_HL}$	OC threshold when high line is detected	Vcomp=upper clamp	1	1.1	1.2	V
Zero Current Detector						
V_{ZCDH}	Upper clamp voltage	I_{ZCD}=0.5mA	5.5	5.7	6.8	V
V_{ZCDL}	Lower clamp voltage	I_{ZCD}=-0.5mA	0.3	0.65	1	V
V_{ZCDA}	Arming voltage(1)			2.1		V
V_{ZCDT}	Triggering voltage(1)			1.6		V
I_{ZCD}	Input bias current	V_{ZCD}=3V			1	μA
I_{ZCD_src}	Source current	VCC=13V, ZCD=0.3V		4.5		mA
I_{ZCD_snk}	Sink current	VCC=13V, ZCD=6.3V		1		mA
V_{ZCD_dis}	ZCD Disable threshold		250	300	350	mV
V_{ZCD_en}	ZCD Enable threshold			400	450	mV
Gate Driver						
V_L	Gate low level	I_{gate}=200mA			1	V
V_H	Gate high level	I_{gate}=200mA	10		13	V
V_{clamp}	Gate clamp voltage	V_{CC}=28V	11	12.5	14	V
T_r	Gate rising time (20% ~80%)	C_{load}=1nF,		40		ns
T_f	Gate falling time (80% ~20%)	C_{load}=1nF		30		ns
Starter						
T_{start}	Start timer period		100	190	230	μs
T_{ss}	Soft start time		6	10	15	ms

Note:
(1) Values are verified by characterization on bench, not tested in production.

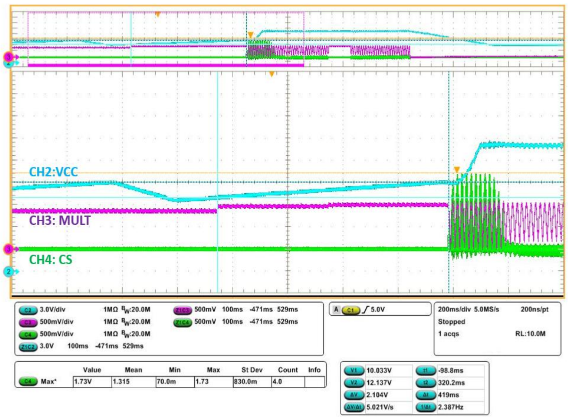
Typical Characteristics



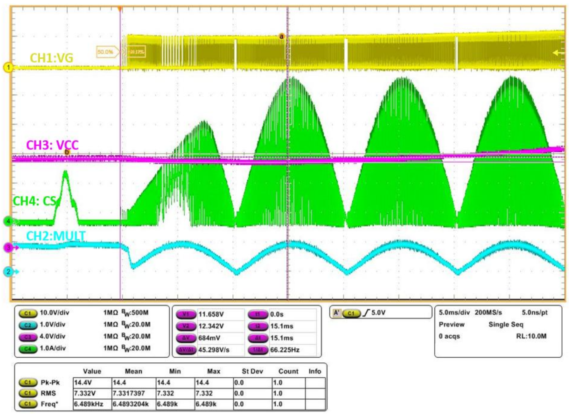
Start-up Current vs Temperature



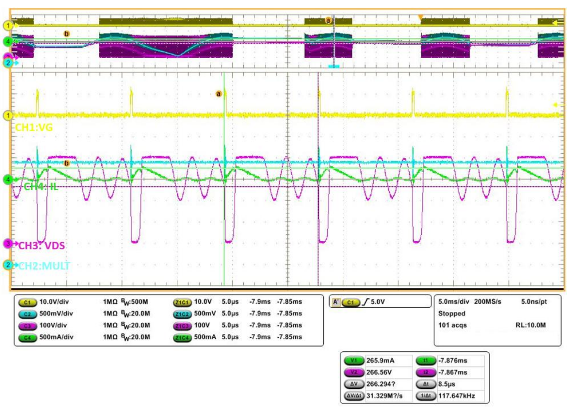
Dynamic OVP Test



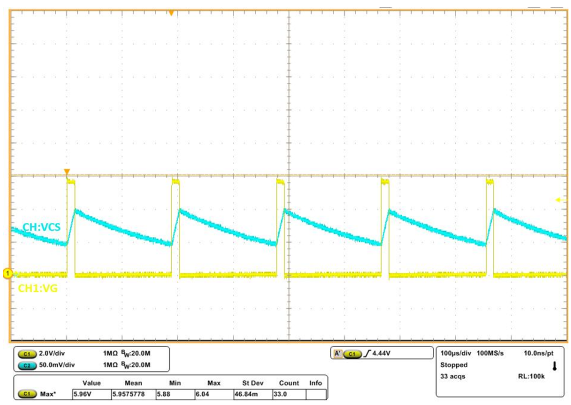
Brown In and Brown Out Test



System Soft Startup Test



Frequency Limit and Valley Switching Test



E-GaN Driver Open Loop Test

Detailed Description

Overview

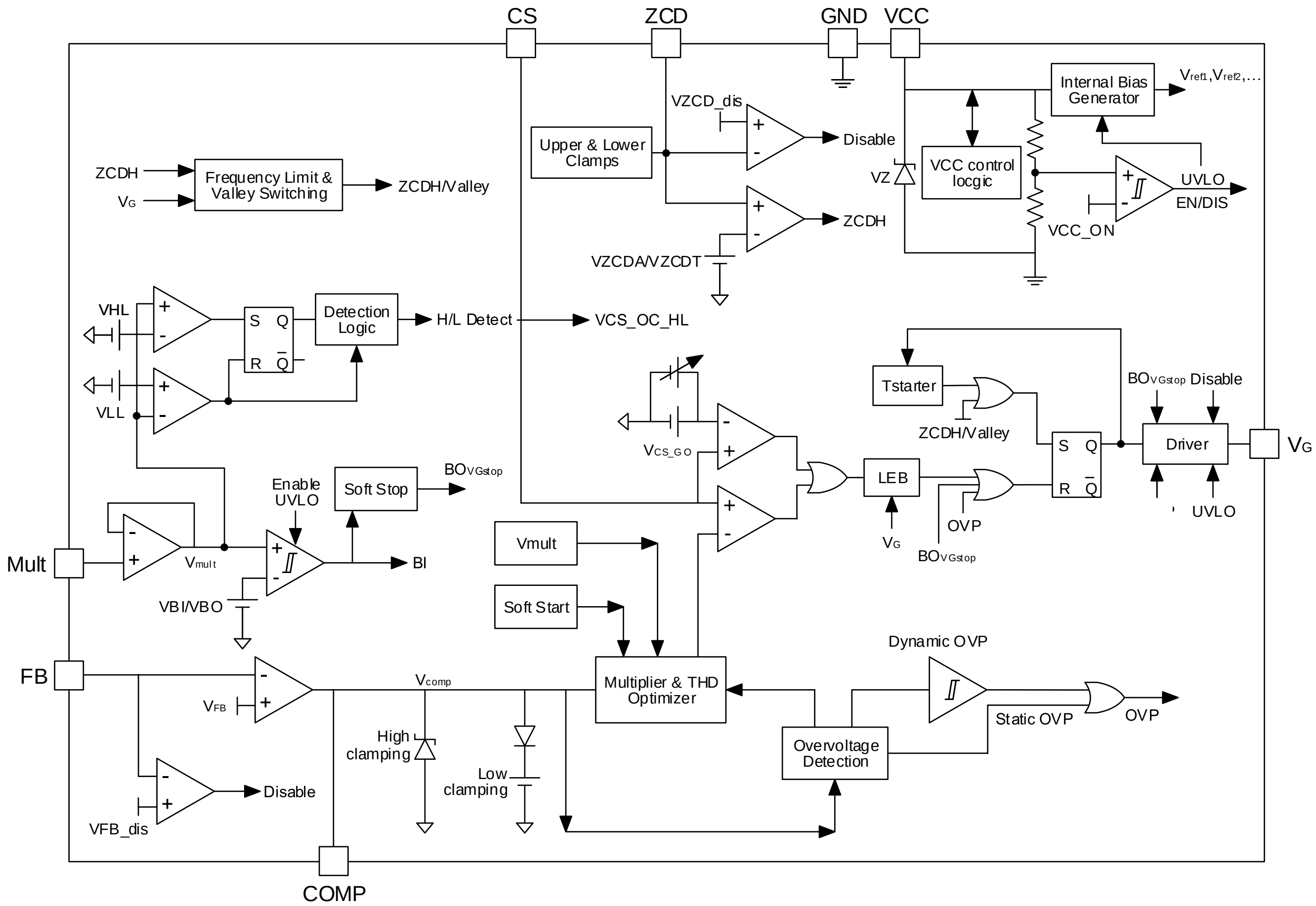
The AS2562 family are critical conduction mode (CrM) power factor correction (PFC) controller for high performance AC/DC power system.，which achieve ultra-low THD and near unity power factor under different operation conditions. This controller is designed for Boost converter operating in critical conduction mode. It features an operational amplifier for feedback error processing, a highly linear multiplier for low THD, a current-sense comparator, a current zero-crossing detector, PWM logic, and a driver for external FET, etc.

The AS2562 is pin compatible with other industrial controllers providing similar functions, while richer enhancement features have been implemented to reduce bill of materials (BOM) cost. The system performance is enhanced by increasing the operating voltage range and optimizing the startup strategy, which makes the controller easier to start in the self-powered system. The device also features innovative dynamic overvoltage protection enhancement circuit, which improves the performance of the system under dynamic load. The soft start function and optimized operating currents of the device result in low current stress and low power consumption. The Intelligent protection functions and strategies of AS2562 can greatly improve system reliability, such as feedback open loop protection, soft stop protection, brown in brown out protection, smart high/low line overcurrent protection.

AS2562 includes a range of features designed to make PFC converter operation well controlled and protected. It can be flexibly configured according to requirements.

Parameter	AS2562
H/L line overcurrent protection	Yes
FB disable function	No
Soft start function	Yes
Brownout protection and soft stop function	Yes
Frequency limit and valley switching	No
Integrated E-GaN Driver	No
Multiplier gain (typ.)	0.6
Current sense reference clamp (typ.)	1.7 V
Dynamic OVP triggering current (typ.)	33 uA
ZCD arm/trigger thresholds (typ.)	2.1/1.6 V

Functional Block Diagram



Feature Description

VCC Power Supply and Undervoltage Lockout

The AS2562 operates from a supply voltage of 11V to 30V. This feature makes AS2562 suitable for a variety of application scenarios. For the best performance, use a typical 0.1uF decoupling capacitor as close as possible between the VCC and GND pins of AS2562. A VCC bypass capacitor (1uF to 10uF) in parallel to the decoupling capacitor is also recommended to reduce noise ripple during switching.

AS2562 has an internal undervoltage lockout (UVLO) protection feature in the VCC supply circuit blocks. When the voltage on the VCC pin exceeds $V_{CC\text{-}ON}$, the controller leaves the UVLO state and activates the SR circuitry. When VCC voltage drops to below $V_{CC\text{-}OFF}$, the controller re-enters the UVLO state.

Disable Function

When FB pin voltage below V_{FB_dis}, shuts down the AS2562 and reduces its consumption at a lower value. To restart the IC, the FB pin voltage must exceed V_{FB_en}. Using this function, user can flexibly control the operating state of the AS2562.

However, it also provides a certain degree of additional security. When the lower resistor of the output voltage divider is shorted to ground or the upper resistor is missing or fails open, the AS2562 will be in the off-protection state. After this, the AS2562 ZCD pin also has similar functions.

Soft Start Function

The output capacitor voltage has not yet been established. When the converter is started or the converter is started with load, it will bring greater current stress to the MOSFET, reducing the reliability of the system. The AS2562 adds a soft start feature. In the start-up stage (T_{SS}), the soft start function is achieved by linearly raising the overcurrent protection threshold. The conduction current on the MOSFET rises steadily.

Overvoltage Function

When the output voltage is higher than the set overvoltage protection point， the difference current will flow through the compensation network and enter the error amplifier output (pin COMP). This current is monitored inside the device. As the current exceeds I_{OVP}, the OVP is triggered (Dynamic OVP).

When the load of a PFC converter is very low, the output voltage tends to stay steadily above the nominal value, which cannot be handled by the Dynamic OVP. If this occurs, however, the error amplifier output will saturate low, when this is detected, the external power transistor is switched off and the AS2562 put in an idle state (Static OVP).

When the system performs a load jump, the AS2562 also adds dynamic overvoltage protection enhancement optimization, which can make the drive waveform as continuous as possible. This improves system noise and ripple. The control diagram is shown on Figure 1.

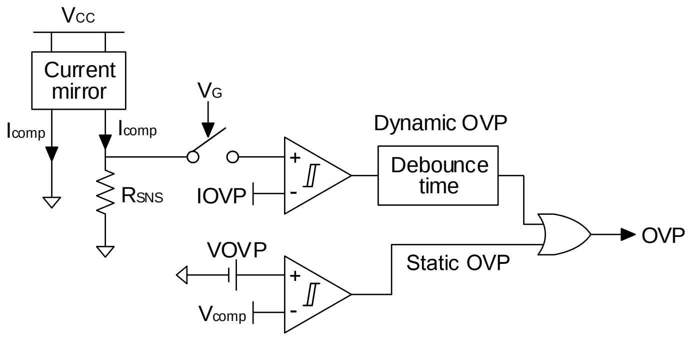


Figure 1. Overvoltage Function Logic Control Diagram

Overcurrent Protection

Under certain conditions (such as inrush, brownout-recovery, and output over-load) the PFC power stage sees large currents. It is critical that the power devices be protected from switching during these conditions.

A shunt resistor in series with MOSFET source leg is used to sense the peak currents. When the MOSFET is turned on, the conduction current flows through the detection resistor, the voltage at the resistor is higher than V_{CS_OC}, the MOSFET is turned off, the AS2562 triggers overcurrent protection. The reference voltage for overcurrent detection in traditional controllers is always a fixed value. However, when the system input voltage changes and the detection resistance is fixed, this can lead to changes in the actual overcurrent protection point. Consequently, under high input voltage, MOSFETs may be damaged due to overcurrent, and the overcurrent protection point has not yet been touched.

AS2562 has improved the above issues by designing a two-level overcurrent protection threshold based on the input voltage. When the voltage of the MULT pin is lower than V_{LL}, AS2562 determines that it is low line, and the overcurrent protection threshold is $V_{CS\_OC\_LL}$. When the voltage of the MULT pin is higher than V_{HL}, it is judged as high line and the overcurrent protection threshold is reduced to $V_{CS\_OC\_HL}$. In this way, the AS2562 can effectively solve the problem of high low line overcurrent point differences under wide input voltage conditions. The control diagram is shown on Figure 2.

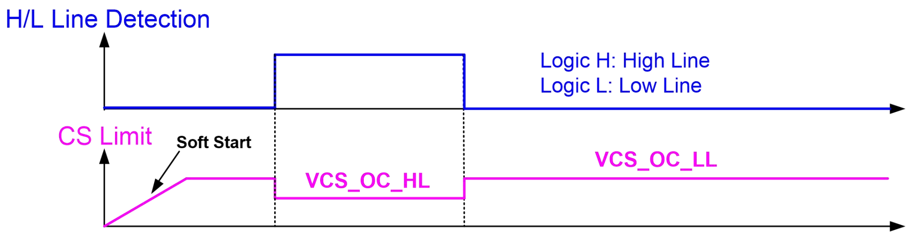


Figure 2. High/Low Line Overcurrent Protection Control Diagram

Brownout Protection and Soft Stop Function

As the power line voltage decreases, input current must increase to maintain a constant output voltage for a specific load. Brownout protection helps prevent excess system thermal stress (due to the higher RMS input current) from exceeding a safe operating level.

Power-line voltage is sensed at MULT pin. When the MULT pin voltage fails to exceed the brownout threshold (V_{BO}), a brownout condition is detected, and gate drive output does not immediately turn off until the input voltage approaches the trough. The addition of the soft stop function ensures a smooth shutdown and does not lead to incorrect startup due to oscillations. During brownout, COMP is actively pulled low, soft-start condition is initiated and the VCC pin continues to sink about 1mA of current until the VCC voltage drops to UVLO. When the MULT pin voltage rises above the brown in threshold (V_{BI}) and VCC pin exceeds $V_{CC\text{-}ON}$, the power stage soft start as COMP rises with controlled voltage. The control diagram is shown on Figure 3.

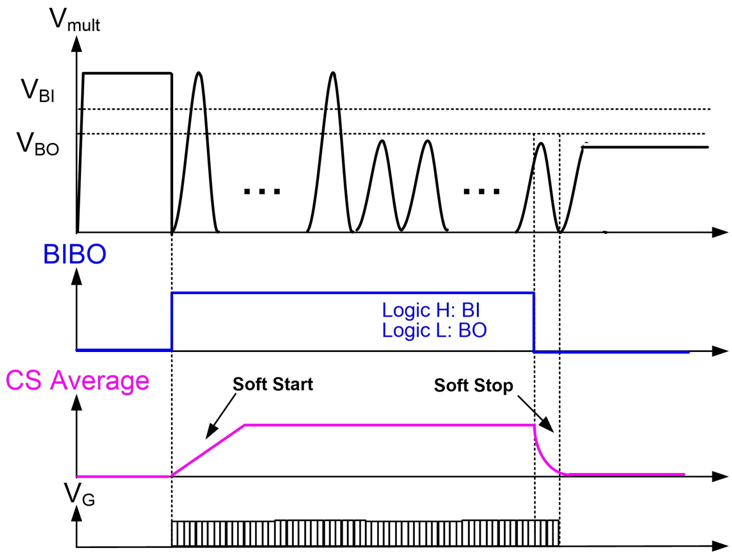


Figure 3. Brownout Protection and Soft Stop Function Control Diagram

Maximum Operating Frequency Limit and Valley Switching

In application scenarios that focus on light-load efficiency, the high switching frequency of CrM increases system switching losses. This loss is difficult to ignore because the system itself is at an extremely light load stage. Traditional controllers only have a frequency limiting function. Although the switching frequency is reduced, the VDS voltage remains high at the moment the MOSFET is turned on, which increases switching loss and reduces system efficiency. The AS2562 can optionally add frequency limiting and valley switching functions.

Due to the addition of the frequency limiting function, the converter will enter the discontinuous conduction mode (DCM). In this mode, when the switching frequency exceeds the frequency clamping threshold, the circuit operates in DCM with valley turn-on. The control diagram is shown on Figure 4. As can be seen in the figure, the system has entered DCM due to a minimum cycle time ($1/F_{sw\_max}$). The driver will turn on the MOSFET, if the minimum cycle time is exceeded and the VDS is detected to be in a trough.

The addition of this function can significantly improve the efficiency of the system under high voltage and light load, but on the contrary, PF and THD will be affected to a certain extent.

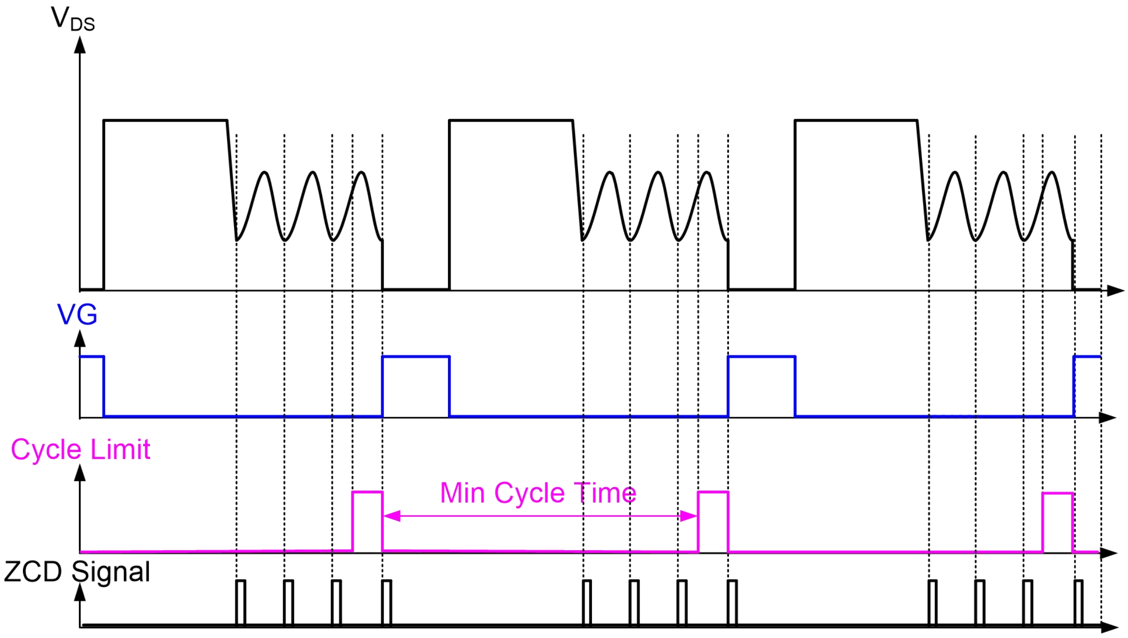


Figure 4. Frequency Limit and Valley Switching Logic Control Diagram

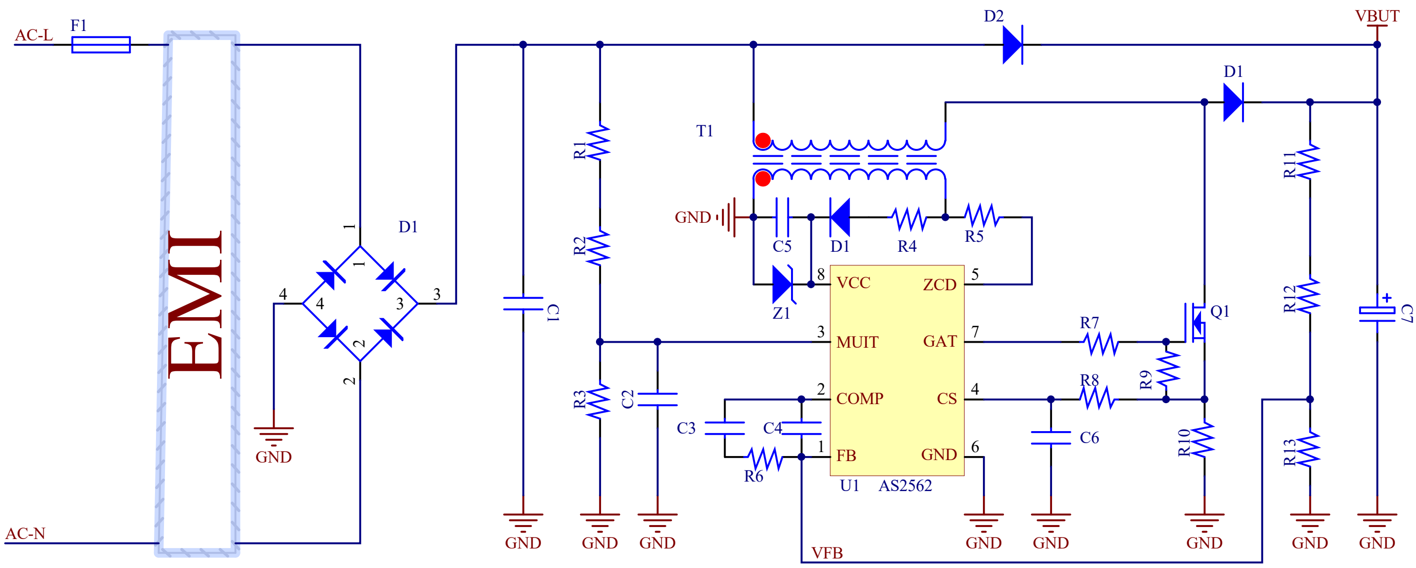
Layout

Layout Guidelines

To achieve high performance of the AS2562, the following layout tips must be followed.

1. Use separate clean traces for VCC and GND pins.
2. At least one low-ESR ceramic bypass capacitor(100nF) must be used. Place the capacitor as close as possible to the AS2562 VCC and GND pins.
3. The GND pin on the ground plane needs to route with a short and wide trace. It is necessary to note that the power GND and signal GND should be routed separately, and a single point of ground should be maintained.
4. In order to minimize interference caused by capacitive coupling of the boost inductor, the device should maintain a distance from the boost inductor. It is also recommended that the device not be placed underneath magnetic elements.
5. Because of the precise zero current detection requirement, the ZCD resistor should be placed as close as possible to the ZCD pin.
6. Keep the loop area between the CS sampling resistor and the CS pin as small as possible.
7. Avoid placing the FB, COMP and MULT traces close to any other high dV/dT traces that would induce significant noise into the high impedance leads.
8. The trace from the VGA pin to the gate of the MOSFET needs to be as short as possible.

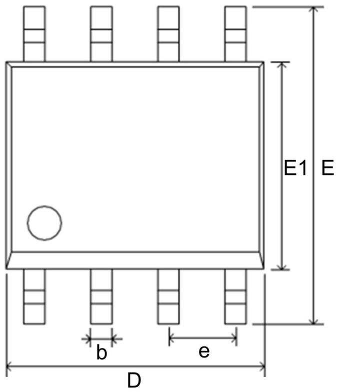
Typical Application



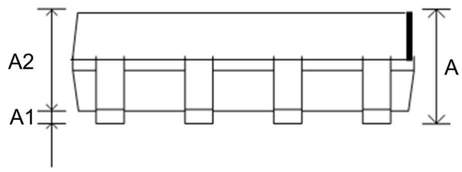
AS2562 Typical Schematic

Package Description

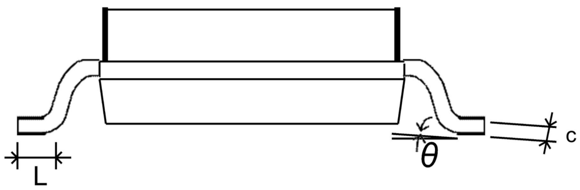
SOP-8



SOP-8 Top View



SOP-8 Side View



SOP-8 Side View

SYMBOL	Millimeter	
	MIN	MAX
A	1.45	1.75
A1	0.10	0.25
A2	1.35	1.55
b	0.33	0.51
c	0.17	0.25
D	4.70	5.10
E	5.80	6.20
E1	3.80	4.00
e	1.270(BSC)	
L	0.40	1.27
θ	0°	8°

NOTES:
1. This drawing is subject to change without notice
2. All linear dimensions are in millimeters.
3. It is recommended that vias under paste be filled, plugged or tented.