24V electronic fuse with adjustable overvoltage protection

General Description

The AS25947 family of electronic fuses are highly integrated circuit protection and power management solutions in small packages. The device uses very few external components and offers multiple protection modes. They are effective against overloads, short circuits, voltage surges, excessive inrush currents and reverse currents. The current limit level can be programmed with an external resistor. An internal circuit will off the internal FET to protect overvoltage. Applications with special voltage ramp requirements can use a single capacitor to program dVdT to ensure the proper output ramp rate.

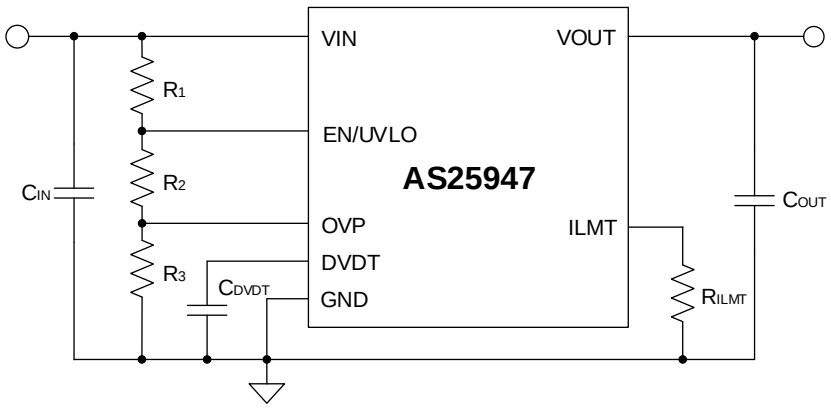
Features

- Operating input voltage range VIN: 4.5V~24V
- Integrated 28mΩ MOS Field Effect Transistor
- 1.34V Reference for Overvoltage protection
- 1A to 5A Adjustable Current I_{ILMT}
- Programmable OUT slew rate, undervoltage lockout (UVLO)
- Built-in thermal shutdown
- DFN3*3-10 & ESOP-8

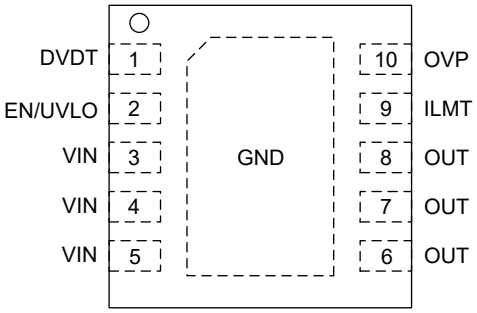
Applications

- Adapter powered devices
- Hard Disk Drives (HDD) and Solid State Drives (SSD)
- Set-top box
- Server/auxiliary (AUX) power
- Fan control
- PCI/PCIe cards

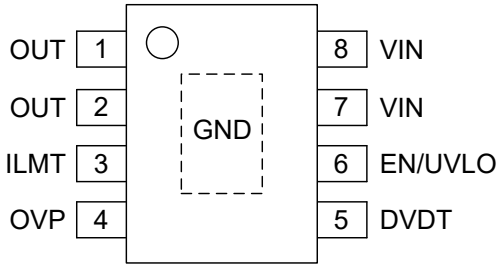
Typical Application Circuit



Pin Configuration



DFN3*3-10



ESOP-8

Pin Descriptions

PIN NO.		PIN name	Description
DFN3*3	ESOP8		
1	5	dVdT	Tie a capacitor from this pin to GND to control the ramp rate of OUT at device turn-on.
2	6	EN/UVLO	This is a dual function control pin. When used as an ENABLE pin and pulled down, it shuts off the internal pass MOSFET. As an UVLO pin, it can be used to program different UVLO trip point via external resistor divider.
3~5	7,8	VIN	Input supply voltage
6~8	1,2	OUT	Output of the device
9	3	ILMT	A resistor from this pin to GND will set the overload and short circuit limit.
10	4	OVP	External over voltage protection via resistor divider. The reference voltage is 1.34V (typical).
Thermal Pad		GND	Ground

Ordering Information

PART No.	PACKAGE	Logo	Tape&Reel
AS25947	ESOP-8	AS25947	3000pcs/reel
AS25947D	DFN3*3-10	AS25947D	3000pcs/reel

Recommended operating condition

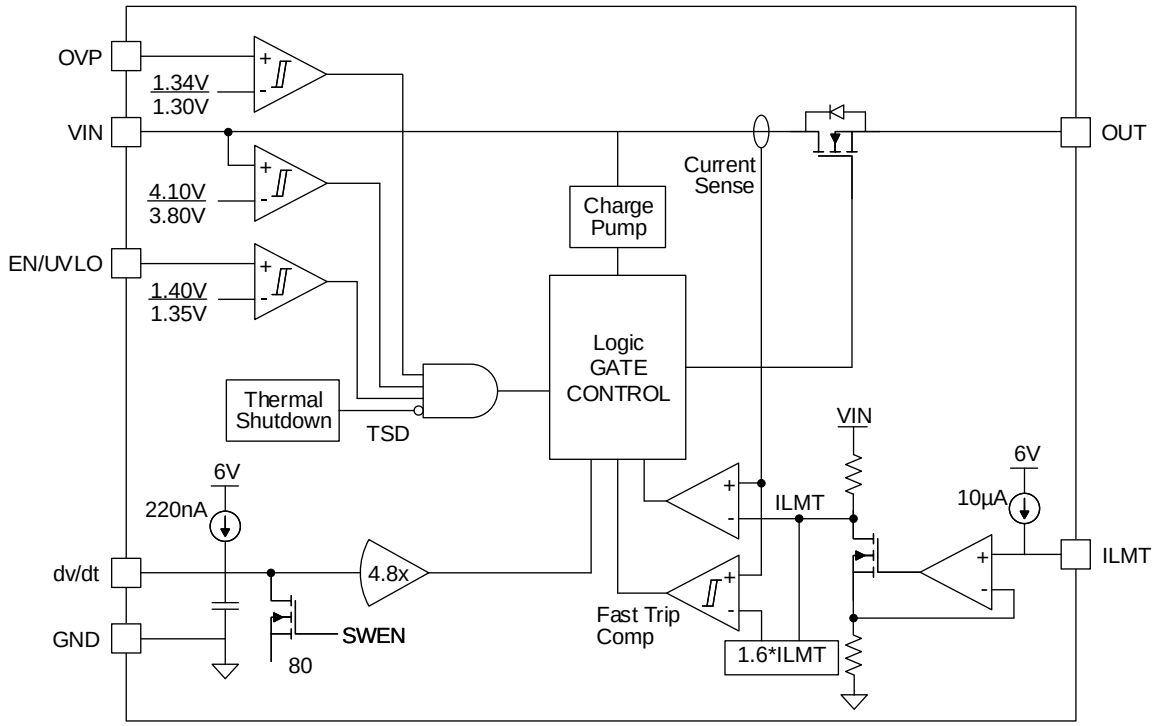
Symbol	Rating	Unit
VIN	4.5 to 24	V
dVdT, EN/UVLO, OVP	0 to 6	V
ILMT	0 to 3	V
I_{OUT}	0 to 4	A
Ambient temperature	-40~85	°C
Operating temperature	-40~125	°C

Absolute Maximum ratings

Parameter	Value	Unit
VIN	-0.3 to 30	V
VIN (10ms Transient)	33(max)	V
OUT	-0.3 to VIN+0.3	V
IOUT	5	A
EN/UVLO, dVdT, OVP, ILMT	-0.3 to 7	V
BFET	-0.3 to 40	V
Junction temperature	150	°C
Storage temperature, T_{stg}	-55 to 150	°C
Leading temperature (soldering, 10secs)	260	°C
ESD Susceptibility HBM	±2000	V

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

BLOCK DIAGRAM



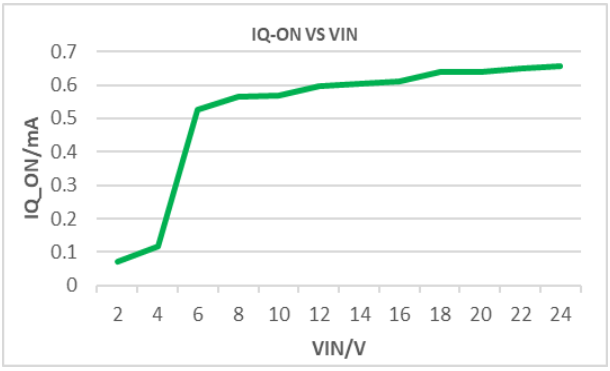
Electrical characteristics

(V_{IN}=12V, $V_{EN/UVLO}$=2V, R_{ILMT} = 10kΩ, C_{dVdT} = OPEN. T_A = 25°C, unless otherwise noted)

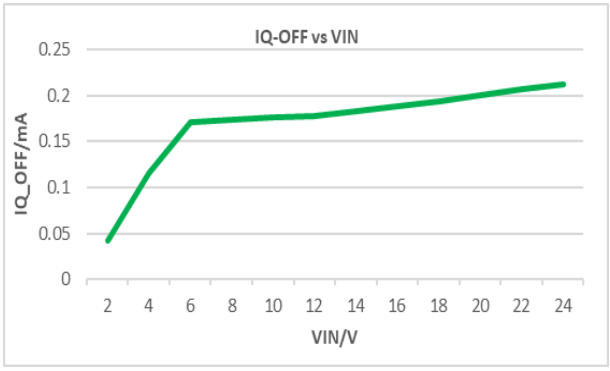
Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
VIN PIN						
VUVO	UVLO threshold, rising		3.80	4.10	4.60	V
	UVLO threshold, falling		3.60	3.80	4.40	V
IQ_{ON}	Supply current	Enabled: EN/UVLO = 2V	0.30	0.60	0.90	mA
IQ_{OFF}		EN/UVLO = 0V	0.10	0.18	0.30	
EN/UVLO						
V_{ENR}	EN Threshold voltage, rising		1.20	1.40	1.60	V
V_{ENF}	EN Threshold voltage, falling		1.15	1.35	1.50	V
I_{EN}	EN Input leakage current	0V ≤ V_{EN} ≤ 5V	-100	0.45	100	nA
dVdT						
I_{dVdT}	dVdT Charging current		100	250	350	nA
R_{dVdT_disch}	dVdT Discharging resistance		50	85	120	Ω
$V_{dVdTmax}$	dVdT max capacitor voltage			5.5		V
$GAIN_{dVdT}$	dVdT to OUT gain			4.85		V/V
ILMT						
I_{ILMT}	ILMT Bias current		0.2	0.7	2.2	μA
I_{OL}	Overload current limit	R_{ILMT} = 4.3kΩ, $V_{VIN-OUT}$ = 1V	4.6	5	5.6	A
		R_{ILMT} = 10kΩ, $V_{VIN-OUT}$ = 1V	2.5	3.0	3.5	A
		R_{ILMT} = 51kΩ, $V_{VIN-OUT}$ = 1V	1.0	1.5	2.0	A
		R_{ILMT} = 100kΩ, $V_{VIN-OUT}$ = 1V	0.8	1.0	1.5	A
$I_{OL-R-Short}$	Overload current limit	R_{ILMT} = 0Ω, Shorted Resistor Current Limit		1.8		A
$I_{OL-R-Open}$	Overload current limit	R_{ILMT} = OPEN, Open Resistor Current Limit		1.6		A
I_{SCL}	Short-circuit current limit	R_{ILMT} = 5kΩ, $V_{VIN-OUT}$ = 12V	4.0	4.25	4.5	A
		R_{ILMT} = 10kΩ, $V_{VIN-OUT}$ = 12V	2.76	2.88	3.0	
		R_{ILMT} = 51kΩ, $V_{VIN-OUT}$ = 12V	1.06	1.14	1.22	
		R_{ILMT} = 100kΩ, $V_{VIN-OUT}$ = 12V	0.86	0.94	1.0	
$RATIO_{FASTRIP}$	Fast-Trip comparator level w.r.t. overload current limit	$I_{FASTRIP}$: I_{OL}		160		%
$V_{OpenILMT}$	I_{LMT} open resistor detect threshold	V_{ILMT} Rising, R_{ILMT} = OPEN	2.3	3.2	3.8	V
$R_{DS\ (on)}$	FET ON resistance		20	28	48	mΩ
$I_{OUT-OFF-LKG}$	OUT Bias current in off state	$V_{EN/UVLO}$ = 0V	0	4	6	μA
$I_{OUT-OFF-SINK}$		$V_{EN/UVLO}$ = 0V, V_{OUT} = 300mV (Sinking)	-5	-2.6	0	μA
OVP						
V_{OVPR}	External OVP threshold	OVP rising	1.30	1.34	1.38	V
V_{OVPF}	External OVP threshold	OVP falling	1.25	1.30	1.35	V
TSD						
T_{SHDN}	TSD Threshold, rising			135		°C
$T_{SHDNhyst}$	TSD Hysteresis			-10		°C
Timing Requirements						
T_{ON}	Turn-on delay	EN/UVLO → H to I_{IN} = 100mA, 1A resistive load at OUT		900		μs
t_{OFFdly}	Turn Off delay			20		μs
dVdT						
t_{dVdT}	Output ramp time	EN/UVLO → H to OUT = 11.7V, C_{dVdT} = 0		1		ms
		EN/UVLO → H to OUT = 11.7V, C_{dVdT} = 1nF		10		ms
ILMT						
$t_{FastOffDly}$	Fast-Trip comparator delay	I_{OUT} > $I_{FASTRIP}$ to I_{OUT}= 0 (Switch Off)		350		ns

Characteristic plots

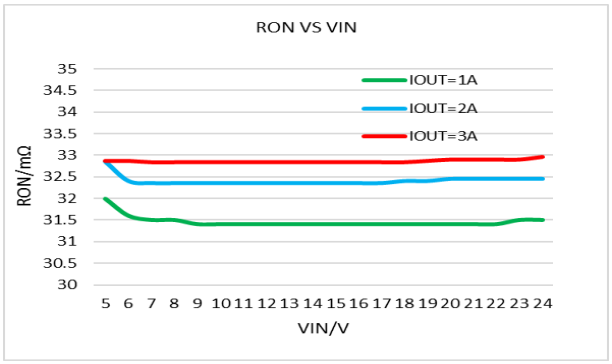
VIN = 12V, $V_{EN/UVLO}$ = 2V, R_{ILMT} = 10kΩ, C_{IN} = 0.1μF, C_{OUT} = 1μF, C_{dVdT} = 1nF (unless stated otherwise)



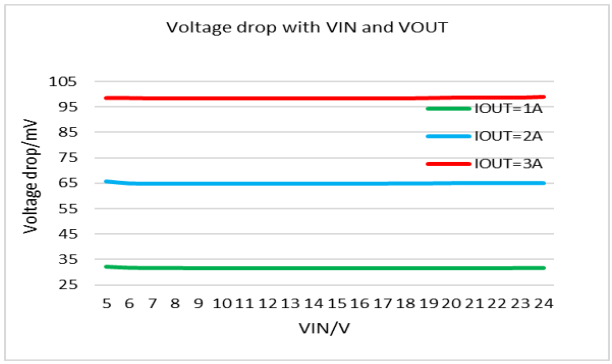
IQ-ON vs VIN



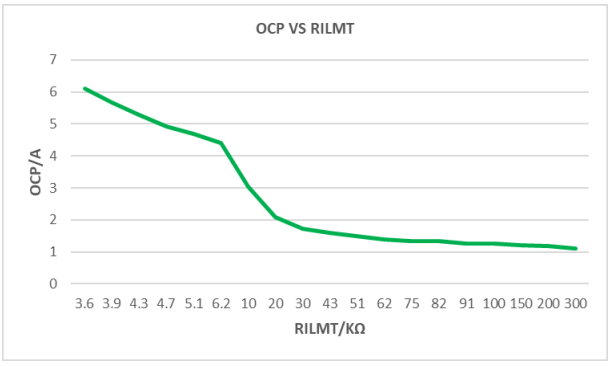
IQ-Off vs VIN



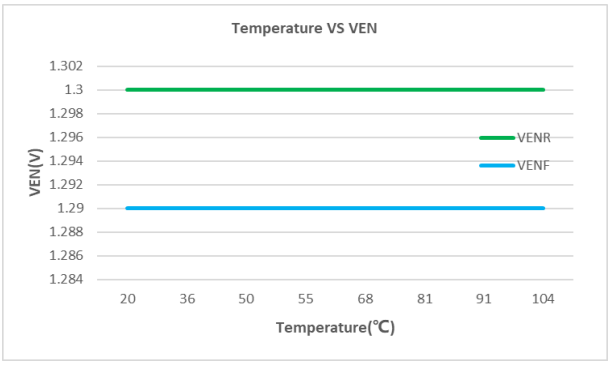
Internal on resistance vs VIN



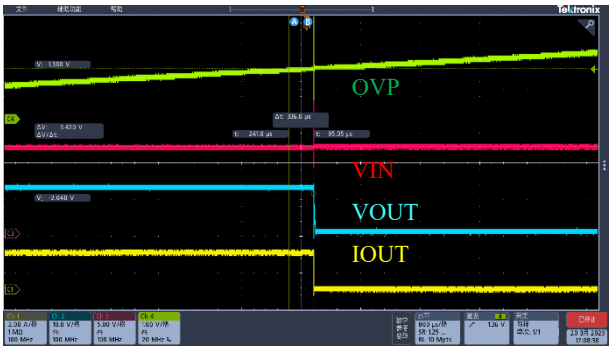
Voltage drops between VIN and VOUT



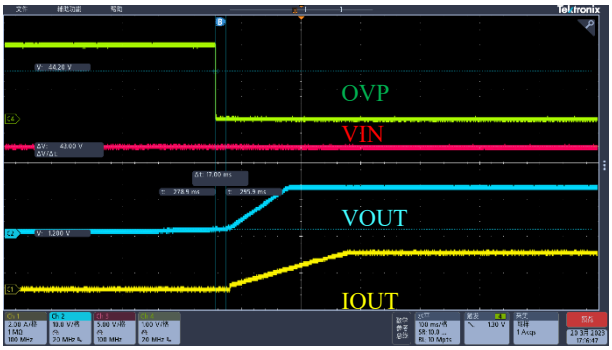
OCP vs RILMT



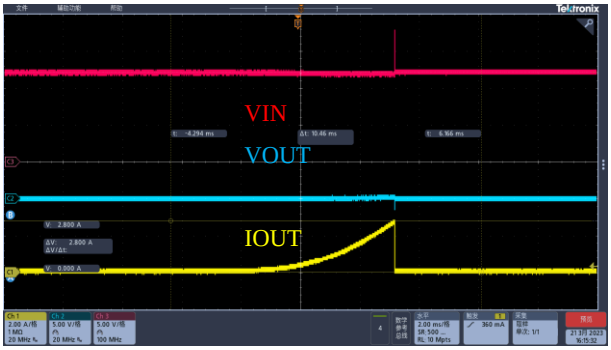
EN vs Temperature



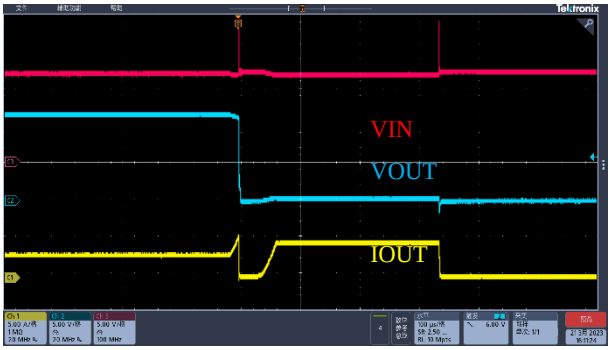
Input over voltage protection



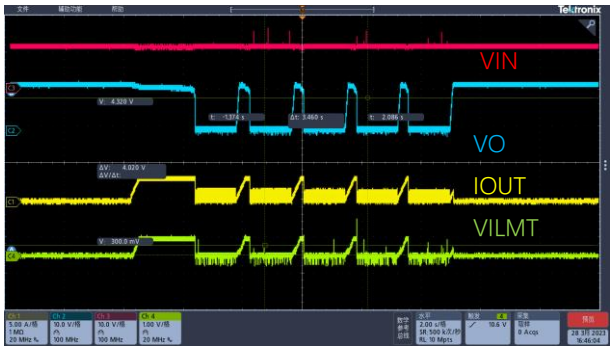
Input over voltage protection release



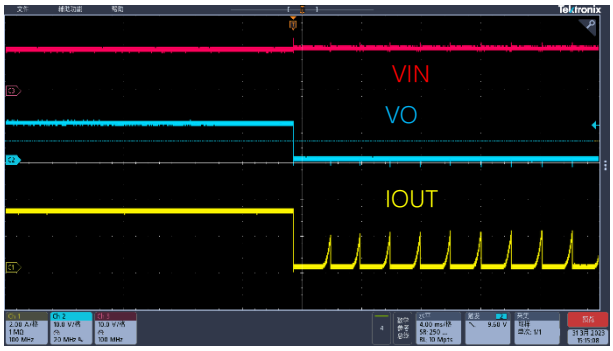
Output short circuit protection in startup



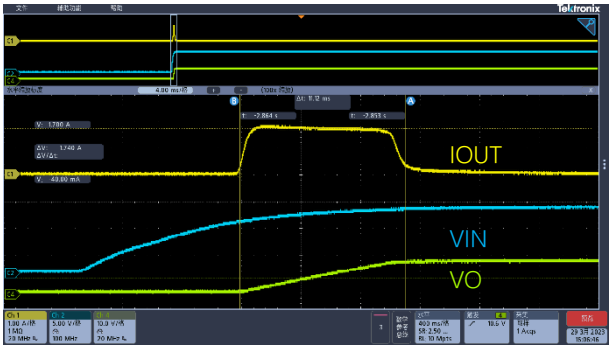
Output short circuit protection in normal operation



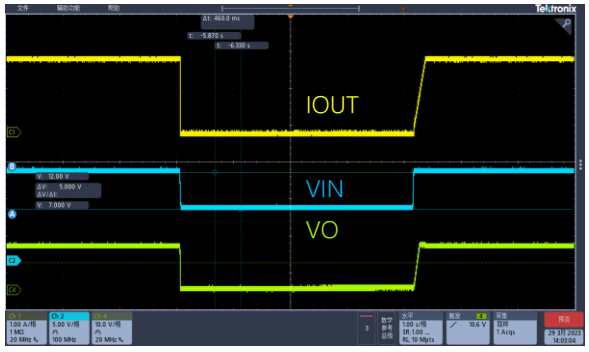
Over current protection and release



Thermal fault auto-retry



Hot plug



Input undervoltage protection and release

Operation Description

The AS25947 is an e-fuse with integrated power switch that is used to manage current/voltage/start-up voltage ramp to a connected load. The device starts its operation by monitoring the VIN bus. When VIN exceeds the undervoltage-lockout threshold (V_{UVR}), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET. As VIN rises, the internal MOSFET of the device will start conducting and allow current to flow from VIN to OUT. When EN/UVLO is held low (below V_{ENF}), internal MOSFET is turned off.

After a successful start-up sequence, the device now actively monitors its load current and input voltage, ensuring that the adjustable overload current limit I_{OL} is not exceeded, and input voltage spikes are safely clamped to V_{OVC} level at the output. This keeps the output device safe from harmful voltage and current transients. The device also has built-in thermal sensor. In the event device temperature (T_J) exceeds T_{SHDN}, typically 135°C, the thermal shutdown circuitry will shut down the internal MOSFET thereby disconnecting the load from the supply. The AS25947 device will remain off during a cooling period until device temperature falls below T_{SHDN} - 10°C, after which it will attempt to restart. This ON and OFF cycle will continue until fault is cleared.

VIN Pin

Input voltage to the AS25947. A ceramic bypass capacitor close to the device from VIN to GND is recommended to alleviate bus transients. The recommended operating voltage range is 4.5V to 24V for AS25947. The device can continuously sustain a voltage of 30V on VIN pin. However, above the recommended maximum bus voltage, the device will be in over-voltage protection (OVP) mode, limiting the output voltage to V_{OVC}. The power dissipation in OVP mode is P_{D_OVP} = (V_{IN} - V_{OVC}) x I_{OUT}, which can potentially heat up the device and cause thermal shutdown.

dVdT

Connect a capacitor from this pin to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum T_{dVdT}) on the output. Equation governing slew rate at start-up is shown below:

$$\frac{dV_{OUT}}{dt} = \frac{I_{dVdT} \cdot GAIN_{dVdT}}{C_{dVdT} + C_{INT}}$$

Where:

I_{dVdT} = 220nA (TYP)

C_{INT} = 70pF (TYP)

$GAIN_{dVdT}$ = 4.85

dV_O/dT = Desired output slew rate

The total ramp time (T_{dVdT}) for 0 to VIN can be calculated using the following equation:

$$T_{dVdT} = 10^6 \cdot V_{IN} \cdot (C_{dVdT} + 70pF)$$

OVP

The over voltage protection can be set by a external resistor divider. When the voltage of OVP pin exceed the internal reference voltage (1.34V typical), the internal MOSFET will be turned off quickly. When the voltage of this pin returns to the hysteresis voltage, the internal MOSFET will be reopened after the dVdT time.

EN/UVLO Pin

As an input pin, it controls both the ON/OFF state of the internal MOSFET and that of the external blocking FET. In its high state, the internal MOSFET is enabled, and charging begins for the gate of external FET. A low on this pin will turn off the internal MOSFET and pull the gate of the external FET to GND via the built-in discharge resistor. High and Low levels are specified in the parametric table of the datasheet. The EN/UVLO pin is also used to clear a thermal shutdown latch in the AS25947 by toggling this pin high to low.

The internal de-glitch delay on EN/UVLO falling edge is intentionally kept low (1us typical) for quick detection of power failure. When used with a resistor divider connected between IN, UVLO, OVP and GND pins of the device, power-fail detection on EN/UVLO helps in quick turn-off of the FET driver, thereby stopping the flow of reverse current. For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO to GND.

ILMT Pin

The device continuously monitors the load current and keeps it limited to the value programmed by R_{ILMT}. After start-up event and during normal operation, current limit is set to I_{OL} (over-load current limit).

When power dissipation in the internal MOSFET [$P_D = (V_{IN} – V_{OUT}) \times I_{OUT}$] exceeds 10W, there is a 2%-12% thermal foldback in the current limit value so that I_{OL} drops to I_{SC}. In each of the two modes, MOSFET gate voltage is regulated to throttle short-circuit and overload current flowing to the load. Eventually, the device shuts down due to over temperature. During a transient short circuit event, the current through the device increases very rapidly. The current-limit amplifier cannot respond very quickly to this event due to its limited bandwidth. Therefore, the AS25947 incorporates a fast-trip comparator, which shuts down the pass device very quickly when $I_{OUT} > I_{FASTRIP}$ and terminates the rapid short-circuit peak current. The trip threshold is set to 60% higher than the programmed overload current limit ($I_{FASTRIP}$ = 1.6 x I_{OL}). After the transient short-circuit peak current has been terminated by the fast-trip comparator, the current limit amplifier smoothly regulates the output current to I_{OL}.

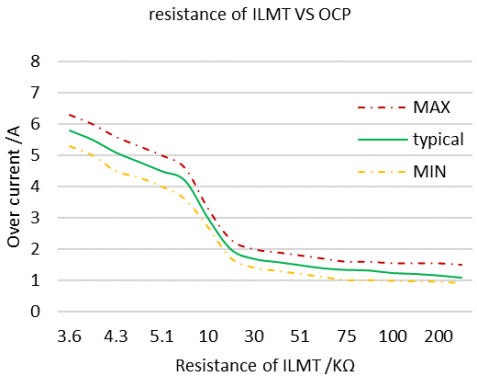
Application and Implementation

Application Information

The AS25947 is a smart eFuse. It is typically used for Hot-Swap and Power rail protection applications. It operates from 4.5V to 18V with programmable current limit and undervoltage protection. The device aids in controlling the in-rush current and provides precise current limiting during overload conditions for systems such as Set-Top-Box, DTVs, Gaming Consoles, SSDs/HDDs, and Smart Meters. The device also provides robust protection for multiple faults on the sub-system rail.

Programming the Current-Limit Threshold: RILMT Selection

The R_{ILMT} resistor at the ILMT pin sets the overload current limit, this can be set using the following table:



Choose closest standard value resistor with 1% tolerance.

Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using an external voltage divider network of R1, R2 and R3 connected between IN, UVLO, OVP and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by the following equation:

$$V_{ENR} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \cdot V_{UV}$$

$$V_{OVPR} = \frac{R_3}{R_1 + R_2 + R_3} \cdot V_{OV}$$

Where V_{ENR} = 1.4V and V_{OVPR} = 1.34V, voltage rising threshold.

Since R_1, R_2 and R_3 will leak the current from input supply VIN, these resistors should be selected based on the acceptable leakage current from input power supply VIN. The current drawn by R_1, R_2 and R_3 from the power supply {I_{R123} = VIN / (R_1 + R_2 + R_3)}.

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, I_{R123} must be chosen to be 20x greater than the leakage current of EN/UVLO and OVP pins.

The power failure threshold is detected on the falling edge of supply. This threshold voltage is 4% lower than the rising threshold, VPFAIL. This is calculated using the following equation.

$$V_{PFAIL} = 0.96 \text{ x } V_{UV}$$

Setting Output Voltage Ramp Time T_{dVdT}

For a successful design, the junction temperature of device should be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The ramp-up capacitor C_{dVdT} needed is calculated considering the two possible cases:

• Start-up without load: only output capacitance C_{OUT} draws current during start-up

During start-up, as the output capacitor charges, the voltage difference as well as the power dissipated across the internal FET decreases. The average power dissipated in the device during start-up is calculated using the following equation.

For AS25947, the inrush current is determined as:

$$I_{INRUSH} = C_{OUT} \cdot \frac{V_{IN}}{T_{dVdT}}$$

Power dissipation during start-up is:

$$P_{D(INRUSH)} = 0.5 \cdot V_{IN} \cdot I_{INRUSH}$$

Equation 8 assumes that load does not draw any current until the output voltage has reached its final value.

• Start-up with load: output capacitance C_{OUT} and load draws current during start-up

When load draws current during the turn-on sequence, there will be additional power dissipated. Considering a resistive load during start-up $R_{L(SU)}$, load current ramps up proportionally with increase in output voltage during T_{dVdT} time. The average power dissipation in the internal FET during charging time due to resistive load is given by:

$$P_{D(LOAD)} = \frac{V_{IN}^2}{6 \cdot R_{L(SU)}}$$

Total power dissipated in the device during startup is:

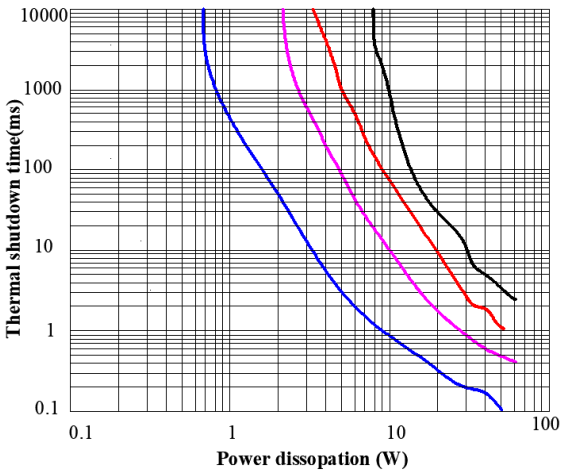
$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)}$$

Total current during startup is given by:

$$I_{STARTUP} = I_{INRUSH} + I_L(t)$$

If $I_{STARTUP}$ > I_{OL}, the device limits the current to I_{OL} and the current limited charging time is determined by:

$$T_{dVdT(Current-limited)} = C_{OUT} \cdot R_{L(SU)} \cdot \left\{ \frac{I_{OL}}{I_{INRUSH}} - 1 + LN\left[\frac{I_{INRUSH}}{I_{OL} - \frac{V_{IN}}{R_{L(SU)}}} \right] \right\}$$



The power dissipation, with and without load, for selected start up time should not exceed the shutdown limits as shown in above figure.

Support Component Selection - C_{IN}

C_{IN} is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range of 0.001μF to 0.1μF is recommended for C_{IN}. If the input supply is located more than a few inches from the device an input ceramic bypass capacitor higher than 0.1μF is recommended.

Power Supply Recommendations

Transient Protection

In case of short circuit and overload current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on value of inductance in series to the input or output of the device. Such transients can exceed the Absolute Maximum Ratings of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

• Minimizing lead length and inductance into and out of the device

• Using large PCB GND plane

• Schottky diode across the output to absorb negative spikes

• A low value ceramic capacitor (C_{IN} = 0.001μF to 0.1μF) to absorb the energy and dampen the transients. The approximate value of input capacitance can be estimated with the following Equation:

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \cdot \sqrt{\frac{L_{IN}}{C_{IN}}}$$

Where:

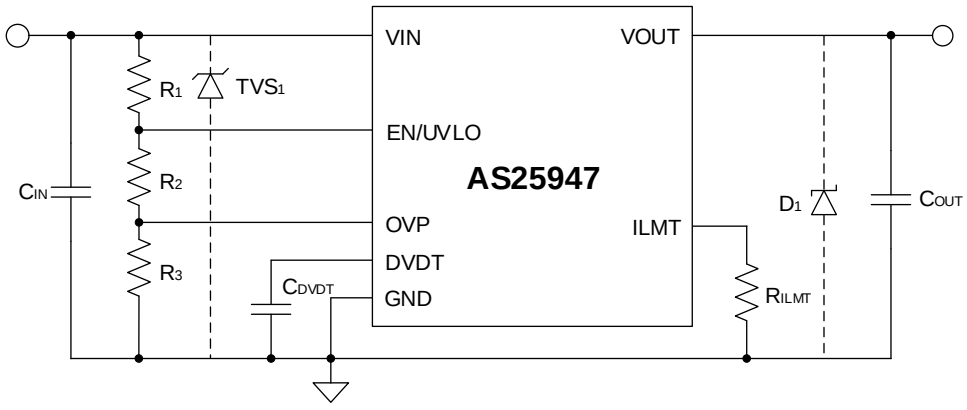
• V_{IN} is the nominal supply voltage

• I_{LOAD} is the load current

• L_{IN} equals the effective inductance seen looking into the source

• C_{IN} is the capacitance present at the input

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the Absolute Maximum Ratings of the device.



Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. Source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the datasheet.

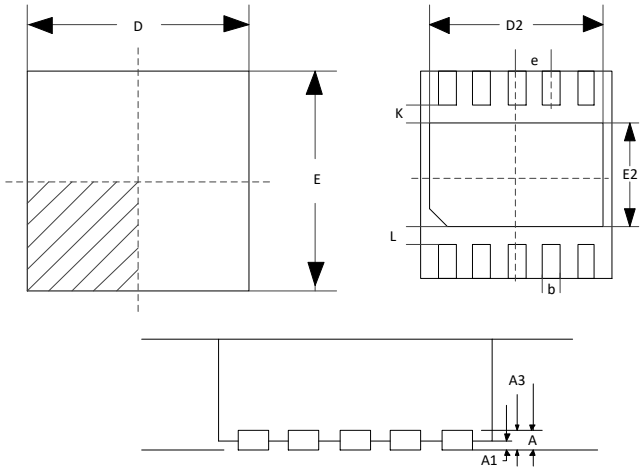
Layout Guidelines

For all applications, a 0.01μF or greater ceramic decoupling capacitor is recommended between IN terminal and GND. For hot-plug applications, where input power path inductance is negligible, this capacitor can be eliminated/minimized.

- The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of AS25947.
- High current carrying power path connections should be as short as possible and should be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of AS25947. The PCB ground should be a copper plane or island on the board.
- Locate all support components: R_{ILMT}, C_{dVdT} and resistors for EN/UVLO and OVP close to their connection pin. Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILMT} and C_{dVdT} components to the device should be as short as possible to reduce parasitic effects on the current limit and soft start timing. These traces should not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes should be placed physically close to the device they are intended to protect and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it should be physically close to the OUT pins.

Package Description

DFN3*3-10



SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.03	0.05
A3		0.20REF	
b	0.18	0.24	0.30
D		3.00BSC	
D2	2.45	2.50	2.55
E		3.00BSC	
E2	1.75	1.80	1.85
e		0.50BSC	
K		0.19TYP	
θ	0.35	0.40	0.45

ESOP-8

Size / Signal	Min	Typ	Max	Size / Signal	Min	Typ	Max
A	4.80		5.00	C	1.30		1.60
A1	0.356		0.456	C1	0.55		0.65
A2	1.27TYP			C2	0.55		0.65
A3	0.345TYP			C3	0.00		0.09
B	3.80		4.00	C4	0.203		0.233
B1	5.80		6.20	D	1.05TYP		
B2	5.00TYP			D1	0.40		0.80
* Unit=mm