High-Side N_MOS Driver and eFuse Solution

General Description

The AS25949 high-side N_FET driver works with an external MOSFET and acts as an ideal diode rectifier when connected in series with the power supply. This controller enables MOSFETs to replace diode rectifiers in power distribution networks, reducing power loss and voltage drop. The AS25949 controller provides charge pump gate drive for an external N-channel MOSFET and fast response comparator to turn off the FET when current flows in reverse.
The current limit in the external series pass N-Channel MOSFET are programmable. The input undervoltage and overvoltage lockout levels are programmabled by resistance divider networks. The AS25949 automatically restarts at a fixed duty cycle. AS25949 is available in 10-pin DFN3*3 and MSOP10L package.

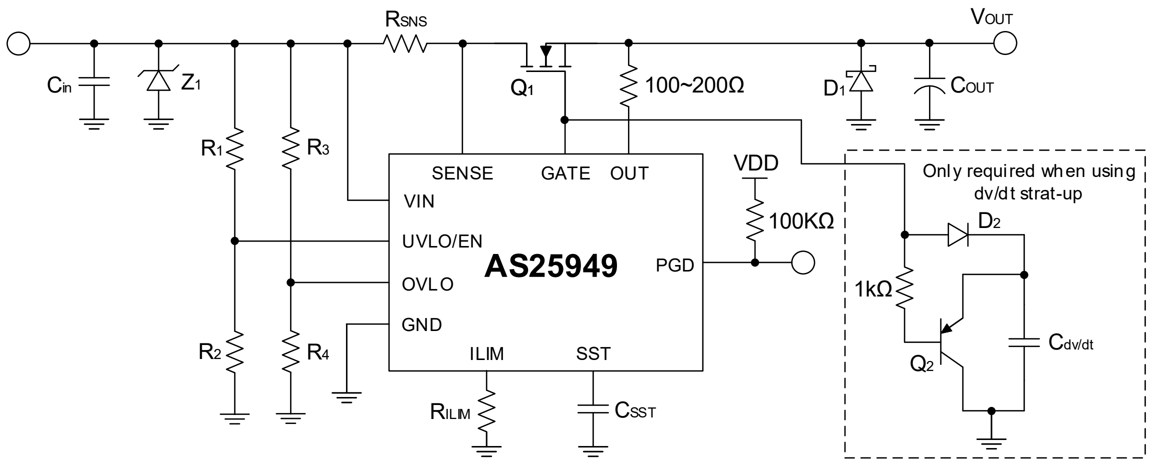
Features

- Wide operating range: 5V to 85V
- Adjustable current limit
- Circuit breaker function for severe overcurrent events
- Internal high side charge pump and gate driver for external N-channel MOSFET
- 50ns fast response to current reversal
- Adjustable undervoltage lockout (UVLO)
- Adjustable overvoltage lockout (OVP)
- Active low open drain POWER GOOD output
- Available with automatic restart
- 10-Pin DFN3*3-10L and MSOP10 package

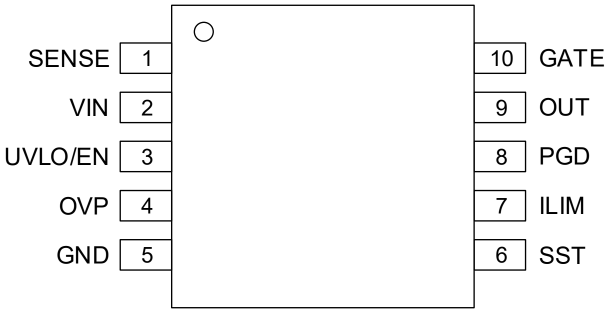
Applications

- Server backplane systems
- Base station power distribution systems
- Solid state circuit breaker
- 24V and 48V Industrial systems

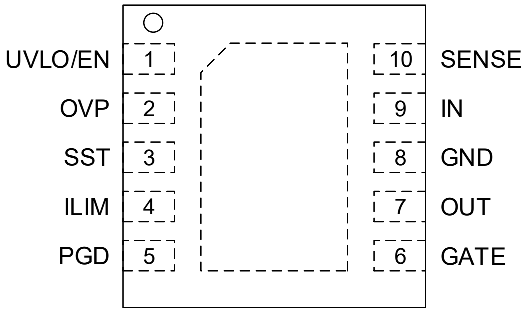
Typical Applications



Pin Configuration



MSOP10



DFN3*3

Pin Descriptions

PIN NO.		PIN name	Description
MSOP10	DFN3*3		
1	10	SENSE	Current sense input: The voltage across the current sense resistor (R_S) is measured from VIN to this pin.
2	9	VIN	Positive supply input: A small ceramic bypass capacitor close to this pin is recommended to suppress transients which occur when the load current is switched off.
3	1	UVLO/EN	This is a dual function control pin. When used as an ENABLE pin and pulled down, it shuts off the internal pass MOSFET. As an UVLO pin, it can be used to program different UVLO trip point via external resistor divider.
4	2	OVP	Overvoltage lockout: An external resistor divider from the system input voltage sets the overvoltage turnoff threshold. The disabled threshold at the pin is 1.23V.
5	8	GND	Circuit ground
6	3	SST	A capacitor from this pin to GND sets output voltage slew rate.
7	4	ILIM	Current limit set: An external resistor connected to this pin, combined with a current detection resistor to achieve overcurrent protection.
8	5	PGD	Power Good indicator: An open drain output.
9	7	OUT	Output feedback: Connect to the output rail (external MOSFET source).
10	6	GATE	Gate drive output: Connect to the external MOSFET's gate. This pin's voltage is typically 12V above the OUT pin when enabled.

Ordering Information

Product model	Packaging form	Smallest packaging	Logo
AS25949	DFN3*3-10L	3000PCS	AS25949
AS25949M	MSOP-10L	3000PCS	AS25949M

Absolute Maximum Ratings

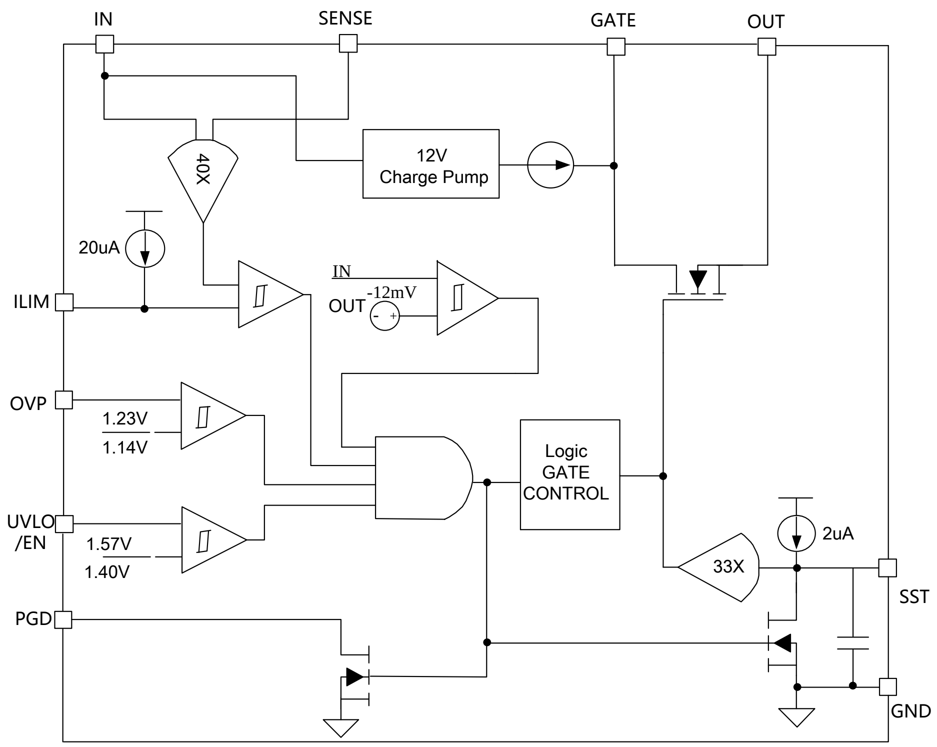
Parameter	Value
VIN to GND	-0.3 to 90V
SENSE, OUT to GND	-0.3 to 90V
GATE to GND	-0.3 to 100V
OUT to GND (1ms transient)	-0.3 to 95V
UVLO to GND	-0.3 to 5.5V
OVP, PGD to GND	-0.3 to 7V
VIN to SENSE	-0.3 to 0.3V
ILIM to GND	-0.3V to 3.5V
Maximum junction temperature, T_{JMAX}	150°C
Storage temperature, T_{stg}	-65 to 150°C

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

Recommended Operating Condition

Symbol	Range
Supply voltage	5 to 85V
PGD off voltage	0 to 5V
ILIM voltage	2.7V max
Junction temperature	-40 to 125°C

Block Diagram

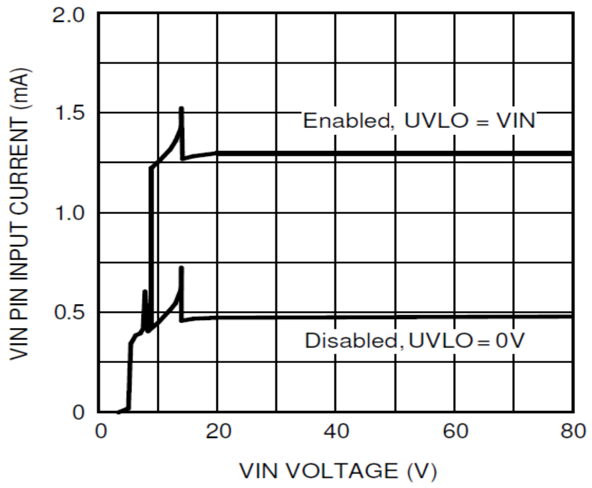


Electrical Characteristics

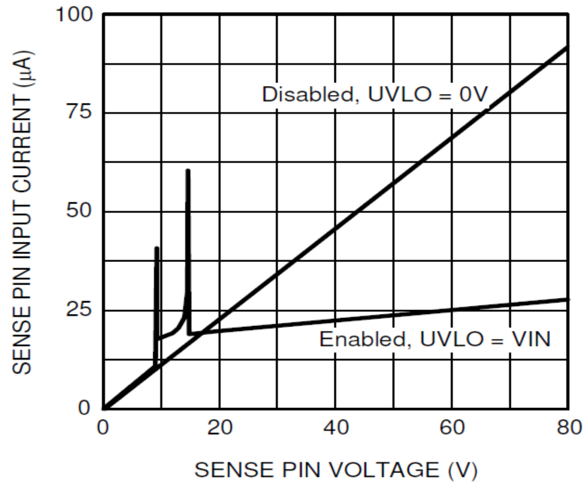
(VIN = 12V, UVLO = 2V, OVP = GND, T_J = 25°C, unless otherwise noted)

Symbol	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT (VIN PIN)						
VIN			5		85	V
IQ_{ON}	Supply current	Enabled: EN/UVLO = 2V	0.50	0.70	0.9	mA
IQ_{OFF}		EN/UVLO = 0V	0.50	0.60	0.70	mA
EN/UVLO						
U_{VLOR}	UVLO Threshold voltage	rising	1.47	1.57	1.67	V
U_{VLOF}	UVLO Threshold voltage	falling	1.30	1.40	1.50	V
I_{UVLO}	UVLO leakage current	EN/UVLO = 0V	-3.5	-2.6	0	uA
t_{DUVLO}	UVLO delay	Delay to GATE high		840		us
		Delay to GATE low		3.4		us
OVP PINS						
V_{OVPR}	OVP Threshold voltage	Rising	1.10	1.23	1.35	V
V_{OVPF}	OVP Threshold voltage	Falling	1.00	1.14	1.30	V
t_{DOVP}	OVP delay	Delay to GATE high		13.8		µs
		Delay to GATE low		4.4		
I_{OVP}	OVP bias current		-1		2	µA
OUT PIN						
I_{OUT-EN}	OUT bias current, enabled	OUT = VIN		10		µA
$I_{OUT-DIS}$	OUT bias current, disabled	Disabled, OUT = 0V, SENSE = VIN	10	20	30	
GATE CONTROL (GATE PIN)						
I_{GATE}	Source current	Normal operation	1	32	40	µA
	Sink current	Disabled	-1	0.1	1	uA
		OVP > 1.23V		2		A
V_{GATE}	Gate output voltage in normal operation	GATE-OUT voltage	8	10	14	V
$V_{SD(REV)}$	Reverse V_{SD} Threshold V_{IN} < V_{OUT}	V_{IN} - V_{OUT}	-55	-12	-1	mV
$t_{SD(REV)}$	Gate turn off time for reverse			36		ns
CURRENT LIMIT						
I_{ILIM}	ILIM Charge current			20		uA
K_A				40		mV/mV
SST (SST PIN)						
I_{SST}	SST Charging current	Normal operation	0	2	5	uA
R_{SST}	SST Discharging resistance		60	75	90	Ω
V_{SSTmax}	SST max capacitor voltage		4.8	5.2	5.5	V
$GAIN_{SST}$	SST to GATE gain			33		V/V
PGD						
V_{PGD}	Output low voltage	I_{SINK} = 10mA	60	75	90	mV
I_{PGD}	Off leakage current	V_{PGD} = 5V	-1	0.5	1	µA

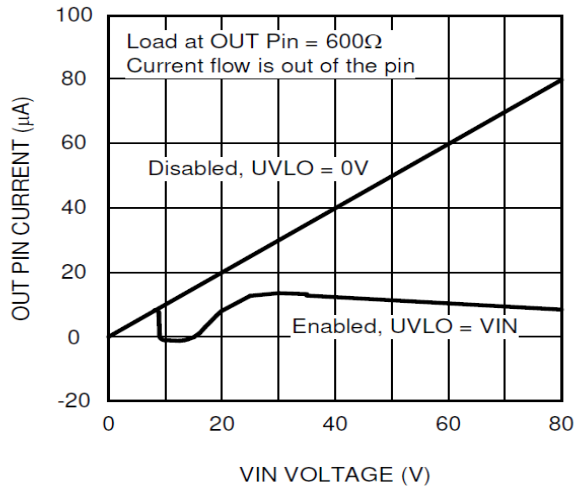
Characteristic Plots



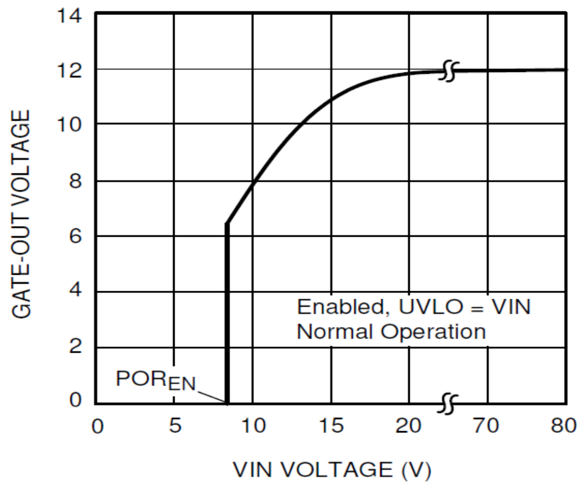
VIN Pin Input Current vs VIN



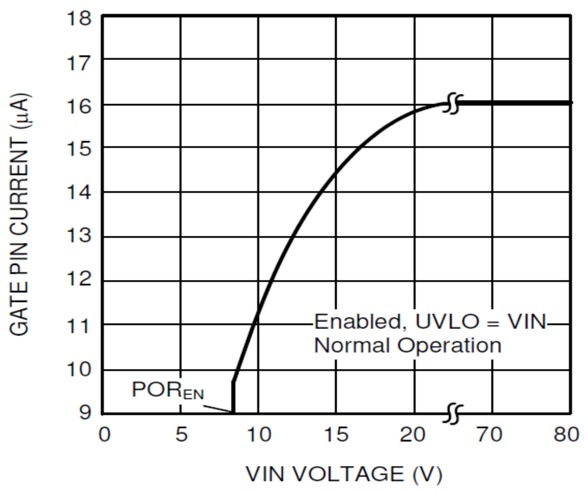
SENSE Pin Input Current



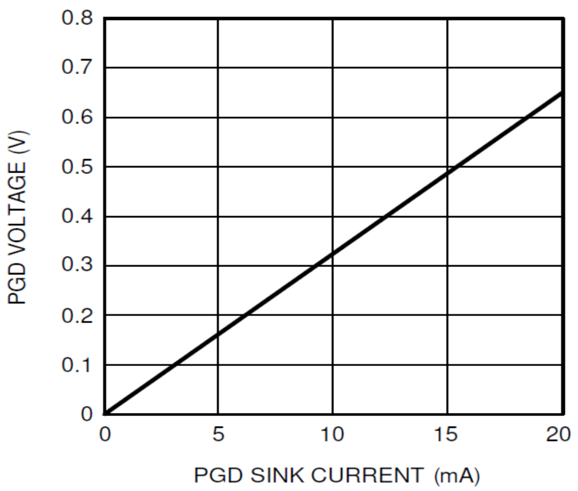
OUT Pin Current



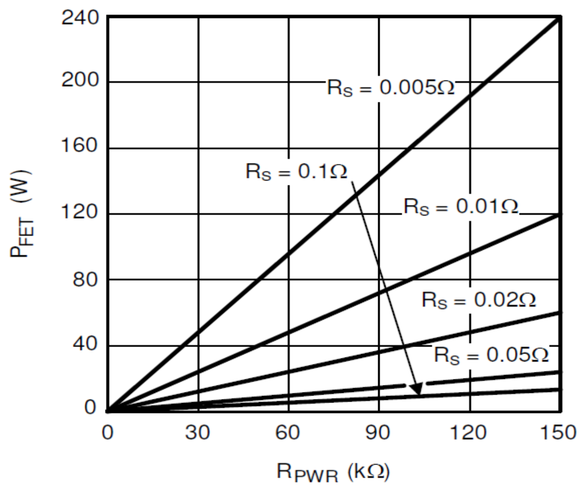
GATE Pin Voltage vs VIN



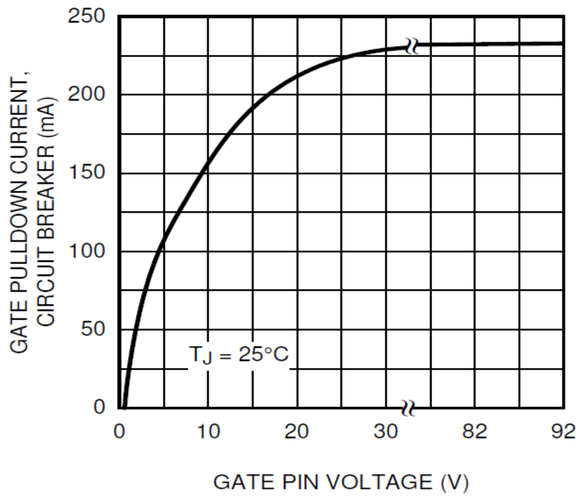
GATE Pin Source Current vs VIN



PGD Pin Low Voltage vs Sink Current



MOSFET Power Dissipation Limit vs RILIM and RS



GATE Pulldown Current, Circuit Breaker vs GATE Voltage

Detailed Description

Overview

AS25949 have programmable current limit, current limiting for an extended period results in the shutdown of the series pass device. In this event, the AS25949 retries an infinite number of times to recover after the fault is removed. The circuit breaker function quickly switches off the series pass device upon detection of a severe overcurrent condition. Programmable undervoltage lockout (UVLO) and overvoltage lockout (OVP) circuits shut down the AS25949 when the system input voltage is outside the desired operating range.

Current Limit

When the voltage across the sense resistor R_S (VIN to SENSE) is multiplied by 40 times reaches the voltage of R_{ILIM}, the overcurrent protection is triggered. In the current limiting condition, the GATE voltage is controlled to limit the current in MOSFET Q1. While the current limit circuit is active, the fault SST is actived. For proper operation, the RS resistor value must be no larger than 100mΩ.

Undervoltage Lockout (UVLO)

As an input pin, it controls the ON/OFF state of the internal MOSFET. In its high state, the internal MOSFET is enabled. A low on this pin will turn off the internal MOSFET. High and Low levels are specified in the parametric table of the datasheet. The EN/UVLO pin is also used to clear a thermal shutdown latch by toggling this pin high to low.

The internal de-glitch delay on EN/UVLO falling edge is intentionally kept low (1us typical) for quick detection of power failure. When used with a resistor divider connected between IN, UVLO, OVP and GND pins of the device, power-fail detection on EN/UVLO helps in quick turn-off of the FET driver, thereby stopping the flow of reverse current. For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO to GND.

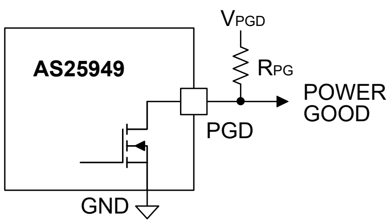
Overvoltage Lockout (OVP)

The over voltage protection can be set by a external resistor divider. When the voltage of OVP pin exceed the internal reference voltage (1.23V typical), the internal MOSFET will be turned off quickly. When the voltage of this pin returns to the hysteresis voltage, the internal MOSFET will be reopened after the dVdT time.

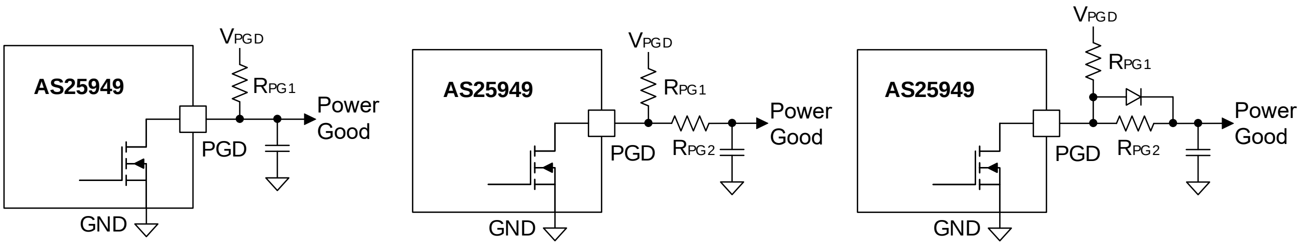
Power Good Pin

During turn-on, the Power Good pin (PGD) is high until the voltage at VIN increases above ≈ 5V. PGD then switches low, remaining low as the VIN voltage increases. When the voltage at OUT increases to within 1.25V of the SENSE pin (VDS <1.25V), PGD switches high. PGD switches low if the VDS of Q1 increases above 2.5V. A pullup resistor is required at PGD as shown in the following figure. The pullup voltage (VPGD) can be as high as 5V.

Power Good Output



If a delay is required at PGD, suggested circuits are shown in the following figure. In figure a), capacitor C_{PG} adds delay to the rising edge, but not to the falling edge. In figure b), the rising edge is delayed by R_{PG1} + R_{PG2} and C_{PG}, while the falling edge is delayed a lesser amount by R_{PG2} and C_{PG}. In figure c), adding a diode across R_{PG2} allows for equal delays at the two edges, or a short delay at the rising edge and a long delay at the falling edge.



a) Delay Rising Edge Only

b) Long delay at rising edge, short delay at falling edge

c) Short Delay at Rising Edge and Long Delay at Falling Edge or Equal Delays

Adding delay to the power good output pin

Gate Control

A charge pump provides internal bias voltage above the output voltage (OUT pin) to enhance the N-Channel MOSFET's gate. The gate-to-source voltage is limited by an internal 12V Zener diode. During normal operating conditions the gate of Q1 is held charged by an internal 32μA current source to approximately 12V above OUT.

Application and Implementation

Design Requirements

When charging the output capacitor through the MOSFET, the FET's total energy dissipation equals the total energy stored in the output capacitor (½CV2). Thus, both the input voltage and output capacitance determine the stress experienced by the MOSFET. The maximum load current drives the current limit and sense resistor selection. In addition, the maximum load current, maximum ambient temperature, and the thermal properties of the PCB (RθCA) drive the selection of the MOSFET RDSON and the number of MOSFETs used. RθCA is a strong function of the layout and the amount of copper that is connected to the drain of the MOSFET. Note that the drain is not electrically connected to the ground plane and thus the ground plane cannot be used to help with heat dissipation. It's a good practice to measure the RθCA of a given design after the physical PCBs are available.

Detailed Design Procedure

Select R_{SNS} and C_L setting

The AS25949 monitors the current in the external MOSFET (Q1) by measuring the voltage across the sense resistor (R_S), connected from VIN to SENSE. The voltage at both ends of the RS is amplified and compared with the voltage at both ends of the R_{ILIM}. If it is greater than the voltage at both ends of the R_{ILIM}, the overcurrent protection is triggered, the gate is pulled to the ground, and external MOSFET is turned off.

Typically sense resistors are only available in discrete value. We choose the next smallest discrete value.

MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous Drain current I_D, the maximum Source current (that is, body diode) IS, the maximum drain-to-source voltage $V_{DS(MAX)}$, the gate-to-source threshold voltage $V_{GS(TH)}$, the drain-to-source reverse breakdown voltage $V_{(BR)DSS}$, and the drain-to-source on resistance $R_{DS(ON)}$.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The rating for the maximum current through the body diode, IS, is typically rated the same as, or slightly higher than the drain current, but body diode current only flows while the MOSFET gate is being charged to $V_{GS(TH)}$.

Gate Charge Time = Qg / $I_{GATE(ON)}$

1. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions.

2. The drain-to-source reverse breakdown voltage, $V_{(BR)DSS}$, may provide some transient protection to the OUT pin in low voltage applications by allowing conduction back to the IN pin during positive transients at the OUT pin.

3. The gate-to-source threshold voltage, $V_{GS(TH)}$, should be compatible with the AS25949 gate drive capabilities. Logic level MOSFETs, with $R_{DS(ON)}$ rated at $V_{GS(TH)}$ at 5V, are recommended, but sub-Logic level MOSFETs having $R_{DS(ON)}$ rated at $V_{GS(TH)}$ at 2.5V, can also be used.

4. The dominate MOSFET loss for the AS25949 active OR-ing controller is conduction loss due to source-to- drain current to the output load, and the $R_{DS(ON)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(ON)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(ON)}$ may not always give desirable results for several reasons:

1. Reverse transition detection. Higher $R_{DS(ON)}$ will provide increased voltage information to the AS25949 Reverse Comparator at a lower reverse current level. This will give an earlier MOSFET turnoff condition should the input voltage become shorted to ground. This will minimize any disturbance of the redundant bus.

2. Reverse current leakage. In cases where multiple input supplies are closely matched it may be possible for some small current to flow continuously through the MOSFET drain to source (that is, reverse) without activating the AS25949 Reverse Comparator. Higher $R_{DS(ON)}$ will reduce this reverse current level.

3. Cost. Generally, as the $R_{DS(ON)}$ rating goes lower, the cost of the MOSFET goes higher.

4. The dominate MOSFET loss for the AS25949 active OR-ing controller is conduction loss due to source-to- drain current to the output load, and the $R_{DS(ON)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(ON)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(ON)}$ may not always give desirable results for several reasons:

a. It is suggested that $R_{DS(ON)}$ be selected to more than 100mV, at the nominal load current.

$$R_{DS(ON)} \leq (100mV / I_D)$$

b. The thermal resistance of the MOSFET package should also be considered against the anticipated dissipation in the MOSFET to ensure that the junction temperature (T_J) is reasonably well controlled, because the $R_{DS(ON)}$ of the MOSFET increases as the junction temperature increases.

$$P_{DISS} = I_D^2 \times (R_{DS(ON)})$$

5. Operating with a maximum ambient temperature ($T_{A(MAX)}$) of 35°C, a load current of 10A, and an $R_{DS(ON)}$ of 10mΩ, and desiring to keep the junction temperature under 100°C, the maximum junction-to-ambient thermal resistance rating ($R\theta_{JA}$) must be:

a. $R_{\theta JA} \leq (T_{J(MAX)} - T_{A(MAX)}) / (I_D^2 \times R_{DS(ON)})$

b. $R_{\theta JA} \leq$ (100°C - 35°C) / (10A × 10A × 0.01Ω)

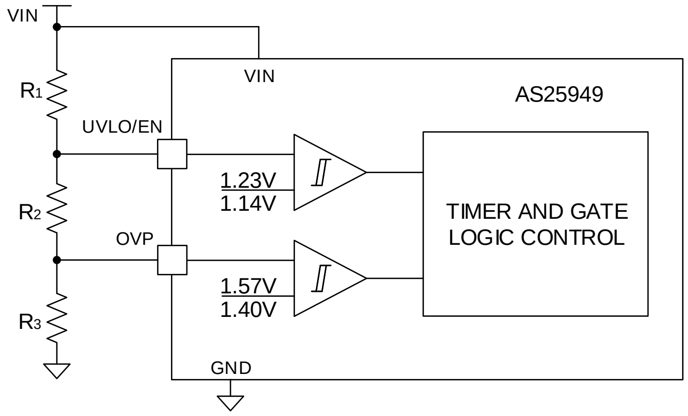
c. $R_{\theta JA} \leq$ 65°C/W.

Set Undervoltage and Overvoltage Threshold

By programming the UVLO and OVP thresholds the AS25949 enables the series pass device (Q1) when the input supply voltage (VIN) is within the desired operational range. If VIN is below the UVLO threshold, or above the OVP threshold, Q1 is switched off, denying power to the load. Hysteresis is provided for each threshold. The OVP function can be disabled by grounding the OVP pin.

Option A

The configuration shown in the following figure requires three resistors (R1 ~ R3) to set the thresholds.



The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using an external voltage divider network of R1, R2 and R3 connected between IN, UVLO, OVP and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by the following equation:

$$V_{UVLOR} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{UVL}$$

$$V_{OVPR} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{OVH}$$

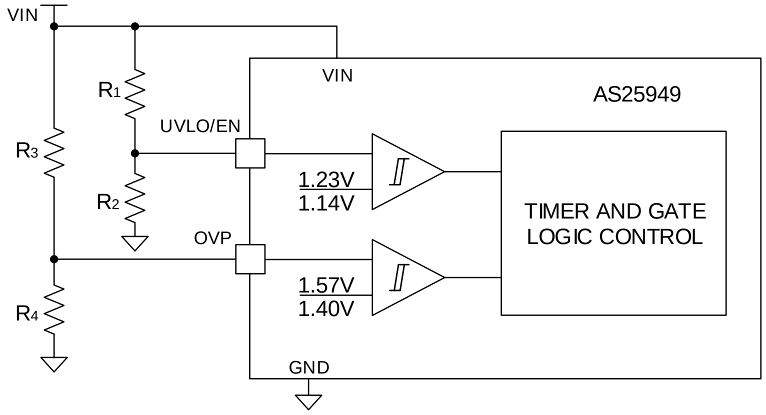
Where V_{UVLOR} = 1.46V and V_{OVPR} = 1.23V.

Since R1, R2 and R3 will leak the current from input supply VIN, these resistors should be selected based on the acceptable leakage current from input power supply VIN. The current drawn by R1, R2 and R3 from the power supply {I_{R123} = VIN / (R1 + R2 + R3)}.

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, I_{R123} must be chosen to be 20x greater than the leakage current of EN/UVLO and OVP pins.

Option B

If all four thresholds must be accurately defined, the configuration in the following figure can be used.



The four resistor values are calculated as follows:

$$R2 = \frac{1.46V \times R1}{V_{UVL} - 1.46V}$$

$$R4 = \frac{1.23V \times R3}{V_{OVH} - 1.23V}$$

Where the R1 ~ R4 resistor values are known, the threshold voltages and hysteresis are calculated by the following equations:

$$V_{UVL} = \frac{1.46V \times (R1 + R2)}{R2}$$

$$V_{OVH} = \frac{1.23V \times (R3 + R4)}{R4}$$

Input and Output Protection

Proper operation of the AS25949 hot swap circuit requires a voltage clamping element present on the supply side of the connector into which the hot swap circuit is plugged in. A TVS is ideal, as depicted in Typical application. The TVS is necessary to absorb the voltage transient generated whenever the hot swap circuit shuts off the load current. This effect is the most severe during a hot-short when a large current is suddenly interrupted when the FET shuts off. The TVS must be chosen to have minimal leakage current at V_{INMAX} and to clamp the voltage to under 30V during hot-short events. A 100~200ohm resistor should be palced between OUT pin and Source of external MOSFET to prevent damage from surge voltage, as the R_{SOURCE} shown in the Typical application.

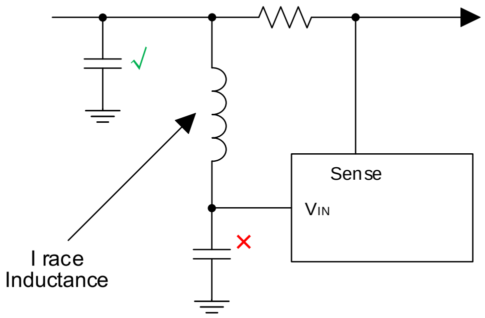
Power Supply Recommendations

In general, the AS25949 behavior is more reliable if it is supplied from a very regulated power supply. However, high-frequency transients on a backplane are not uncommon due to adjacent card insertions or faults. If this is expected in the end system, Maxin recommends placing a 1μF ceramic capacitor to ground close to the drain of the hot swap MOSFET. This reduces the common mode voltage seen by VIN and SENSE. Additional filtering may be necessary to avoid nuisance trips.

Layout Guidelines

The following guidelines must be followed when designing the PC board for the AS25949:

- Place the AS25949 close to the board's input connector to minimize trace inductance from the connector to the FET.
- Note that special care must be taken when placing the bypass capacitor for the VIN pin. During hot shorts, there is a very large dv/dt on input voltage after the MOSFET turns off. If the bypass capacitor is placed right next to the pin and the trace from Rsns to the pin is long, an LC filter is formed. As a result, a large differential voltage can develop between VIN and SENSE. To avoid this, place the bypass capacitor close to Rsns instead of the VIN pin.



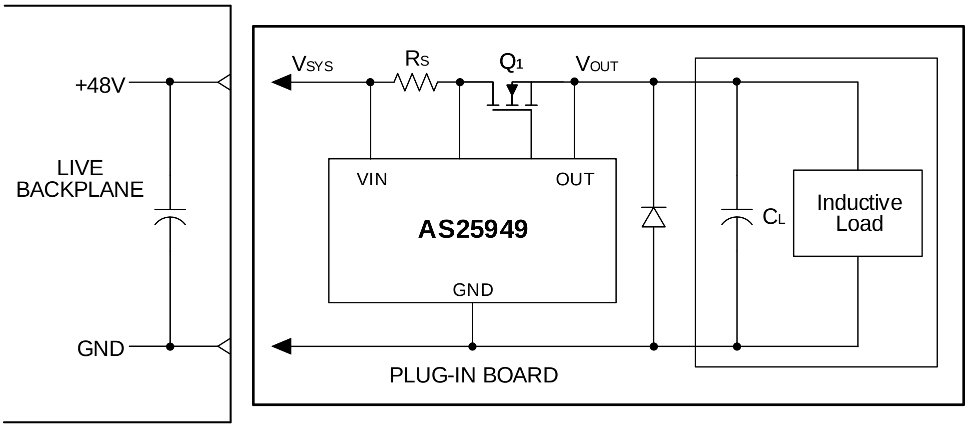
Layout Trace Inductance

- The sense resistor (R_S) must be close to the AS25949, and connected to it using the Kelvin techniques.
- The high current path from the board's input to the load (via Q1), and the return path, must be parallel and close to each other to minimize loop inductance.
- The ground connection for the various components around the AS25949 must be connected directly to each other, and to the AS25949's GND pin, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
- Provide adequate heat sinking for the series pass device (Q1) to help reduce stresses during turnon and turnoff.
- The board's edge connector can be designed to shut off the AS25949 as the board is removed, before the supply voltage is disconnected from the AS25949. When the board is inserted into the edge connector, the system voltage is applied to the AS25949's VIN pin before the UVLO voltage is taken high.

System Considerations

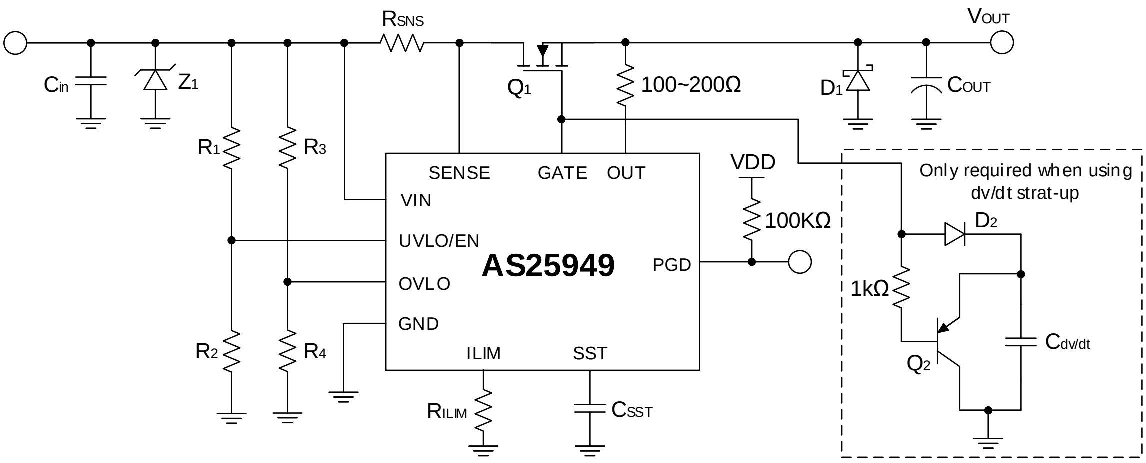
A) Continued proper operation of the AS25949 hot swap circuit requires capacitance be present on the supply side of the connector into which the hot swap circuit is plugged in, as depicted in the following figure. The capacitor in the Live Backplane section is necessary to absorb the transient generated whenever the hot swap circuit shuts off the load current. If the capacitance is not present, inductance in the supply lines generate a voltage transient at shut-off which can exceed the absolute maximum rating of the AS25949, resulting in its destruction.

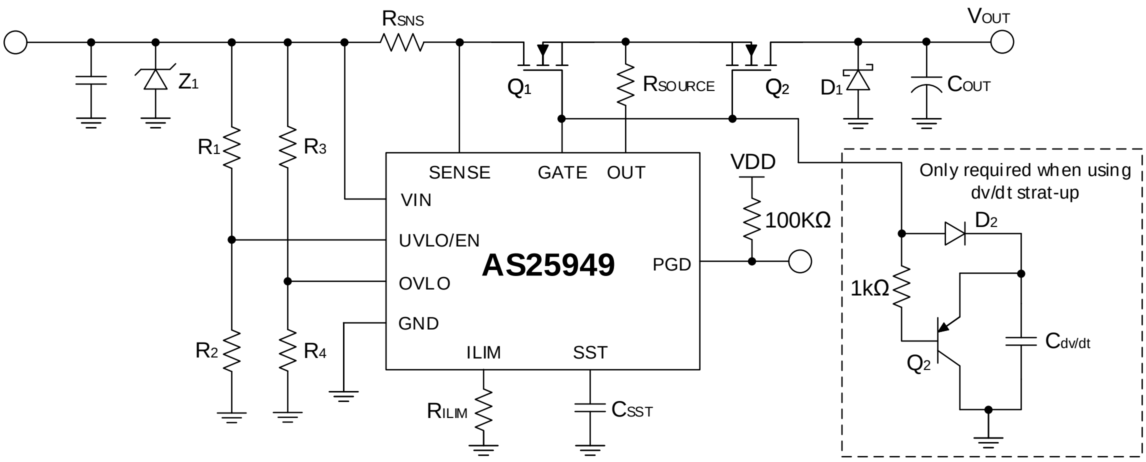
B) If the load powered via the AS25949 hot swap circuit has inductive characteristics, a diode is required across the AS25949's output. The diode provides a recirculating path for the load's current when the AS25949 shuts off that current. Adding the diode prevents possible damage to the AS25949 as the OUT pin is taken below ground by the inductive load at shutoff



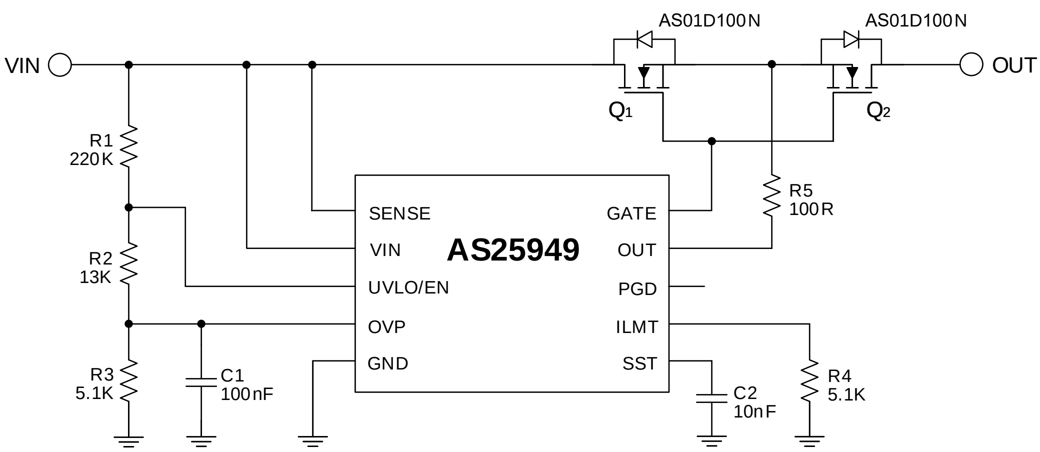
Typical Applications

eFuse Solution



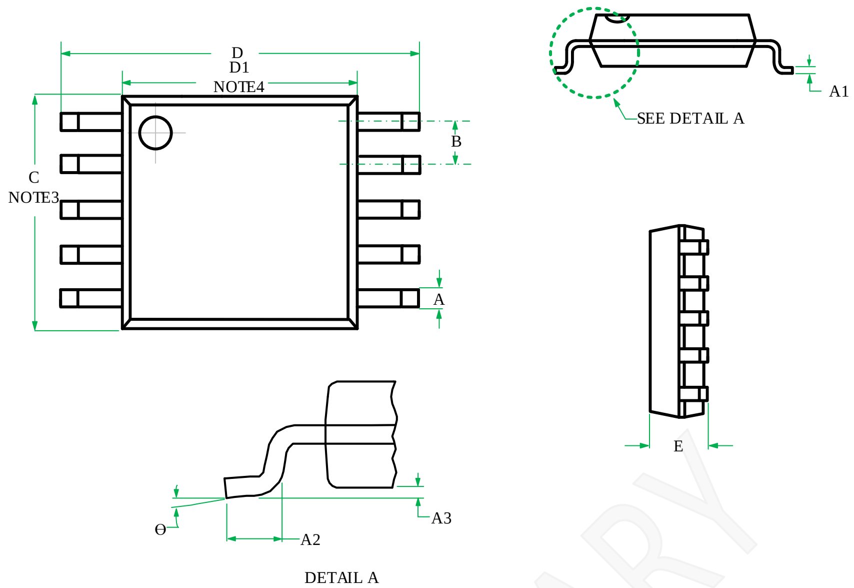


High-Side N_FET Driver



Package Description

MSOP-10L



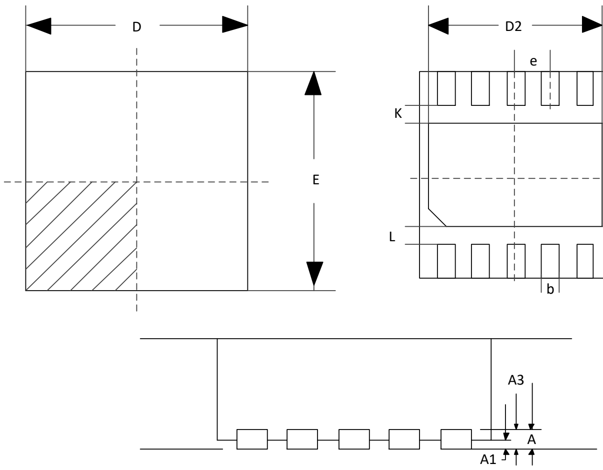
SYMBOL	MILLIMETERS	
	MIN	MAX
A	0.17	0.27
A1	0.13	0.23
A2	0.4	0.7
A3	0.05	0.15
B	0.5typ	
C	2.9	3.1
D	4.75	5.05
D1	2.9	3.1
E	1.1max	
θ	0°	8°

PRELIMINARY

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

DFN3*3-10L



SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.03	0.05
A3	0.20REF		
b	0.18	0.24	0.30
D	3.00BSC		
D2	2.45	2.50	2.55
E	3.00BSC		
E2	1.75	1.80	1.85
e	0.50BSC		
K	0.19TYP		
θ	0.35	0.40	0.45