

## High-Side OR-ing FET Controller

### General Description

The AS5050 high-side OR-ing FET controller works with an external MOSFET and acts as an ideal diode rectifier when connected in series with the power supply. This ORing controller enables MOSFETs to replace diode rectifiers in power distribution networks, reducing power loss and voltage drop.

The AS5050 controller provides charge pump gate drive for an external N-channel MOSFET and fast response comparator to turn off the FET when current flows in reverse.

The AS5050 can be connected to power supplies from 1V to 60V and can withstand transient voltages up to 60V.

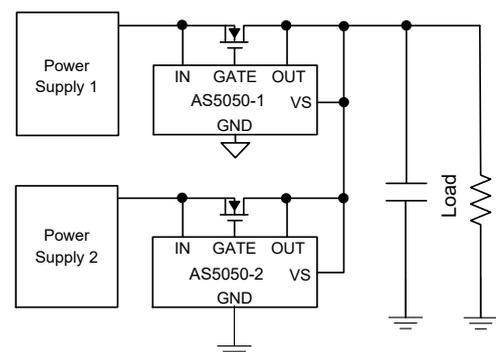
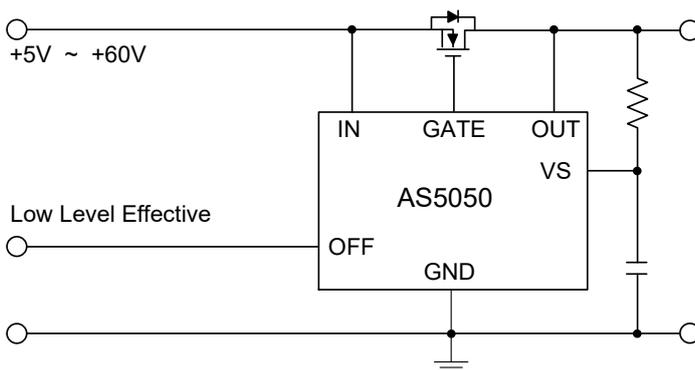
### Features

- Wide operating input voltage range  $V_{IN}$ : 1V to 60V
- 60V transient voltage
- Charge pump gate driver for external N-channel MOSFET
- 50ns fast response to current reversal
- 2A peak gate off current
- Ultra-small VDS turn-off voltage reduces turn-off time
- Available in SOT23-6L and DFN3\*2-8L Package

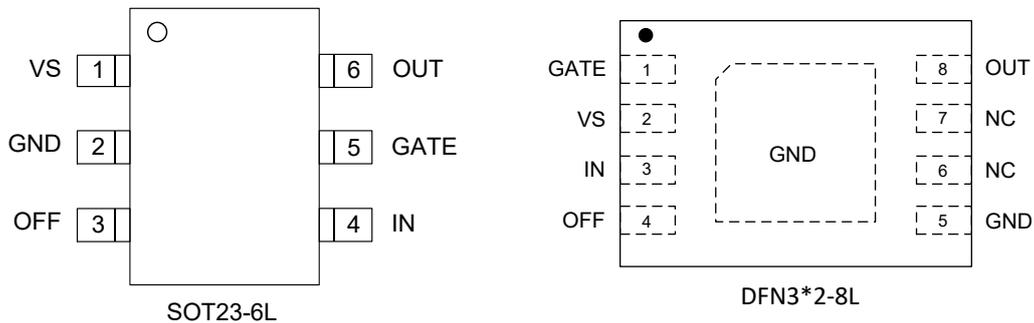
### Applications

- Active OR-ing of redundant (N+1) power supplies

### Typical Application Circuit



## Pin Configuration



## Pin Descriptions

Name	PIN		Description
	SOT23-6	DFN3*2-8L	
GATE	5	1	Connect to the Gate of the external MOSFET. Controls the MOSFET to emulate a low forward- voltage diode.
VS	1	2	The main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump. Typically connected to either VOUT or VIN; a separate supply can also be used.
IN	4	3	Voltage sense connection to the external MOSFET Source pin.
OFF	3	4	A logic high state at the OFF pin will pull the GATE pin low and turn off the external MOSFET. Note that when the MOSFET is off, current will still conduct through the FET's body diode. This pin should may be left open or connected to GND if unused.
GND	2	5, EXP	Ground return for the controller.
NC	/	6, 7	
OUT	6	8	Voltage sense connection to the external MOSFET Drain pin.

## Ordering Information

PART No.	PACKAGE	Tape&Reel
AS5050	SOT23-6	3000pcs/reel
AS5050A	DFN3*2-8L	3000pcs/reel

## Recommended Operating Condition

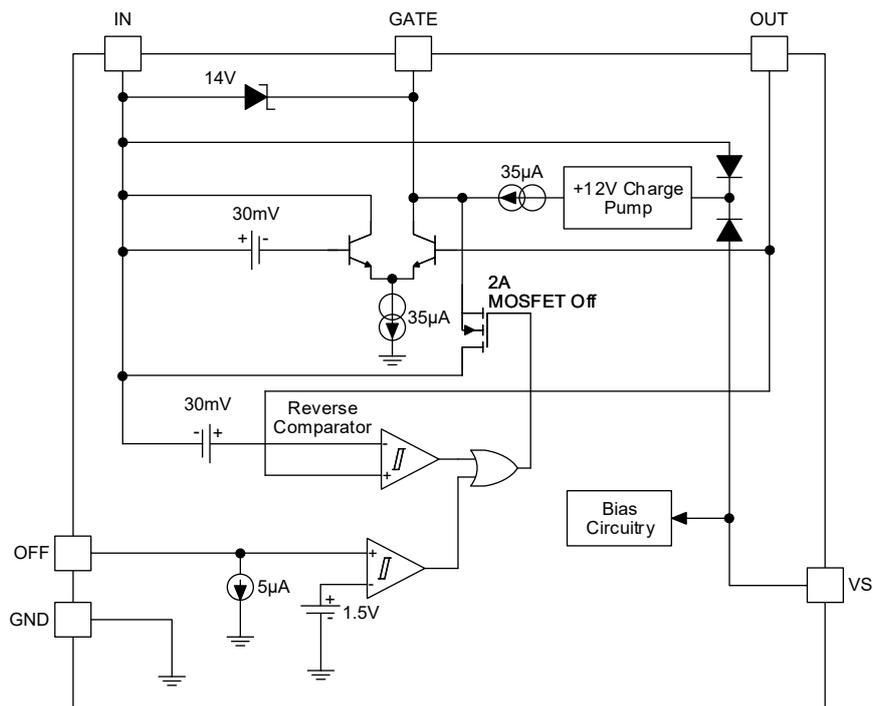
Symbol	Range	Unit
IN, OUT, VS Pins	1-50	V
OFF Pin	0-5.5	V
Junction temperature	-40~125	°C

## Absolute Maximum Ratings

Parameter	Value	Unit
IN, OUT Pins to GND	-0.3 to 60	V
GATE Pin to GND	-0.3 to 60	V
VS Pin to Ground	-0.3 to 60	V
OFF Pin to Ground	-0.3 to 7	V
Junction temperature	150	°C
Storage temperature, Tstg	-55 to 150	°C
Leading temperature (soldering, 10secs)	260	°C
ESD Susceptibility HBM	±2000	V

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

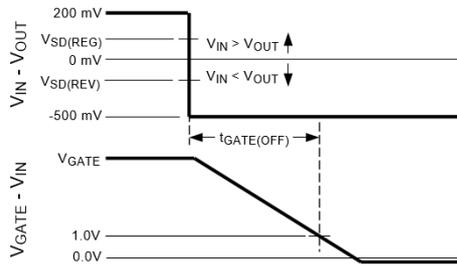
## Block Diagram



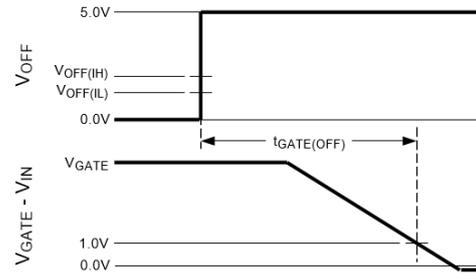
## Electrical Characteristics

( $V_{IN}=12V$ ,  $V_{VS} = V_{IN}$ ,  $V_{OUT} = V_{IN}$ ,  $V_{OFF} = 0V$ ,  $C_{GATE}= 47nF$ ,  $T_A=25^{\circ}C$ , unless otherwise noted)

Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
<b>VS PIN</b>						
$V_{VS}$	Operating Supply Voltage Range		1		60	V
$I_{VS}$	Operating Supply Current	$V_{VS}= 5V, V_{IN} = 5V, V_{OUT} = V_{IN} - 100mV$		75		uA
		$V_{VS}= 12V, V_{IN} = 5V, V_{OUT} = V_{IN} - 100mV$		100		
		$V_{VS}=60V, V_{IN} = 5V, V_{OUT} = V_{IN} - 100mV$		130		
<b>IN PIN</b>						
$V_{IN}$	Operating Input Voltage Range		1		60	V
$I_{IN}$	IN Pin current	$V_{IN}=5V, V_{VS}= V_{IN}, V_{OUT} = V_{IN} - 100mV, GATE = Open$		190		uA
		$V_{IN} = 12V \text{ to } 60V, V_{VS}= V_{IN}, V_{OUT} = V_{IN} - 100mV, GATE = Open$		320		
<b>OUT PIN</b>						
$V_{OUT}$	Operating Output Voltage Range		1		60	V
$I_{OUT}$	OUT Pin Current	$V_{IN} = 5V \text{ to } 60V, V_{VS}= V_{IN}, V_{OUT} = V_{IN} - 100mV$		3.2		uA
<b>GATE PIN</b>						
$I_{GATE(ON)}$	Gate Pin Source Current	$V_{IN} = 5V, V_{VS} = V_{IN}, V_{GATE}=V_{IN}, V_{OUT} = V_{IN} - 175mV$		30		uA
		$V_{IN} = 12V \text{ to } 60V, V_{VS} = V_{IN}, V_{GATE} = V_{IN}, V_{OUT} = V_{IN} - 175mV$		32		
$V_{GS}$	$V_{GATE} - V_{IN}$ in Forward Operation	$V_{IN} = 5V, V_{VS} = V_{IN}, V_{OUT} = V_{IN} - 175mV$		7		V
		$V_{IN} = 12V \text{ to } 60V, V_{VS} = V_{IN}, V_{OUT} = V_{IN} - 175mV$		12		
$t_{GATE(REV)}$	Gate Capacitance Discharge Time at Forward to Reverse Transition	$C_{GATE} = 0$		25		ns
		$C_{GATE} = 10nF$		60		
		$C_{GATE} = 47nF$		180		
$t_{GATE(OFF)}$	Gate Capacitance Discharge Time at OFF pin Low to High Transition	$C_{GATE} = 47nF$		486		ns
$I_{GATE(OFF)}$	Gate Pin Sink Current	$V_{GATE} = V_{IN} + 3V, V_{OUT} > V_{IN} + 100mV, t \leq 10ms$		2.8		A
$V_{SD(REV)}$	Reverse $V_{SD}$ Threshold $V_{IN} < V_{OUT}$	$V_{IN} - V_{OUT}$		-28		mV
$\Delta V_{SD(REV)}$	Reverse $V_{SD}$ Hysteresis			10		mV
$V_{SD(REG)}$	Regulated Forward $V_{SD}$ Threshold $V_{IN} > V_{OUT}$	$V_{IN}=5V, V_{VS} = V_{IN}, V_{IN} - V_{OUT}$		19		mV
		$V_{IN}=12V, V_{VS} = V_{IN}, V_{IN} - V_{OUT}$		22		
<b>OFF PIN</b>						
$V_{OFF(IH)}$	OFF Input High Threshold Voltage	$V_{OUT} = V_{IN} - 500mV, V_{OFF}$ Rising		1.56		V
$V_{OFF(IL)}$	OFF Input Low Threshold Voltage	$V_{OUT} = V_{IN} - 500mV, V_{OFF}$ Falling		1.4		
$\Delta V_{OFF}$	OFF Threshold Voltage Hysteresis	$V_{OFF(IH)} - V_{OFF(IL)}$		155		mV
$I_{OFF}$	OFF Pin Internal Pulldown	$V_{OFF} = 4.5V$		5		uA
		$V_{OFF} = 5V$		8		



Gate OFF Timing for Forward to Reverse Transition



Gate OFF Timing for OFF Pin Low to High Transition

## Characteristic plots

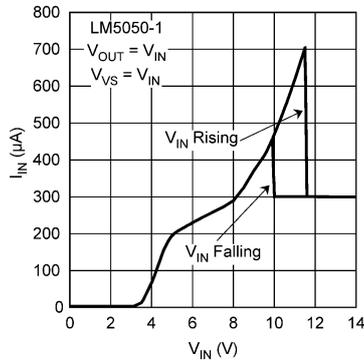


Figure 3.  $I_{IN}$  vs  $V_{IN}$

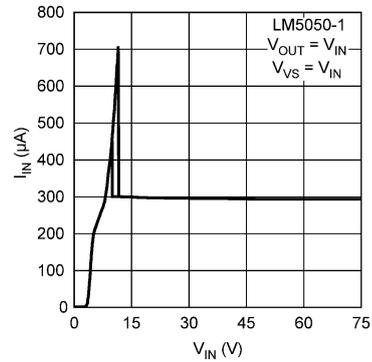


Figure 4.  $I_{IN}$  vs  $V_{IN}$

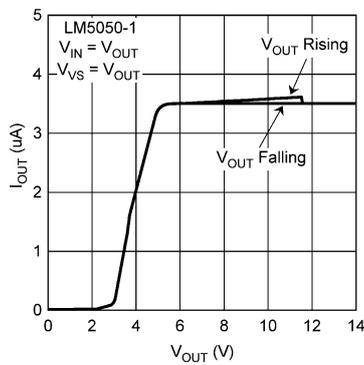


Figure 5.  $I_{OUT}$  vs  $V_{OUT}$

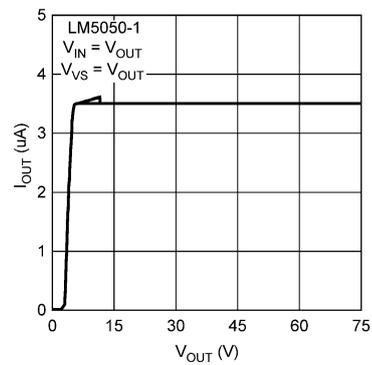


Figure 6.  $I_{OUT}$  vs  $V_{OUT}$

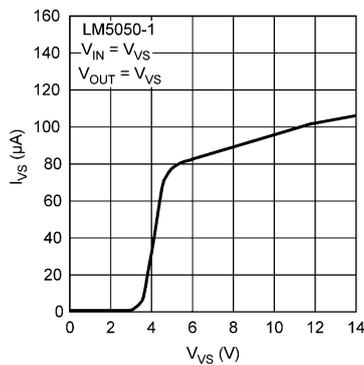


Figure 7.  $I_{VS}$  vs  $V_{VS}$

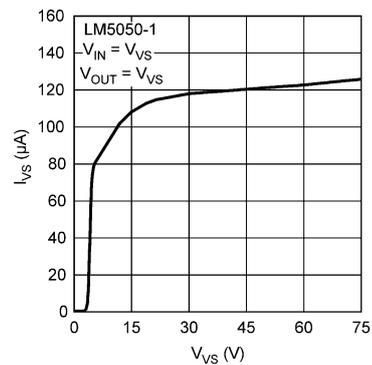


Figure 8.  $I_{VS}$  vs  $V_{VS}$

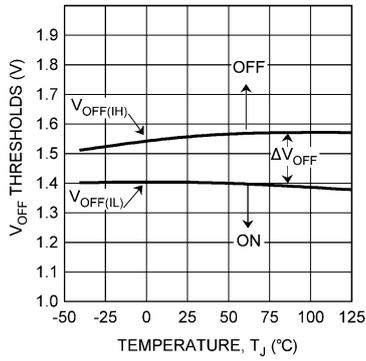


Figure 15. OFF Pin Thresholds vs Temperature

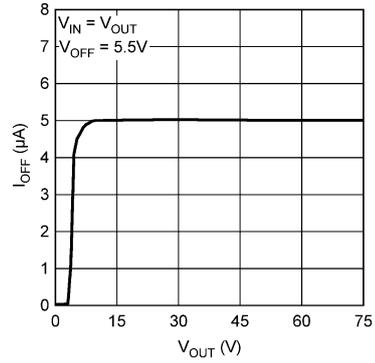


Figure 16. OFF Pin Pulldown vs Temperature

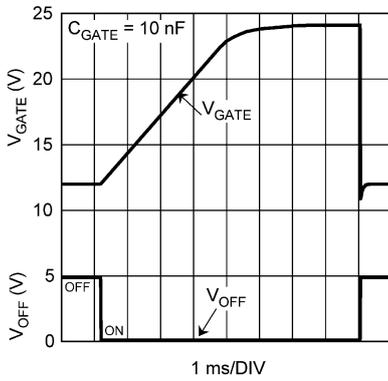


Figure 17.  $C_{GATE}$  Charge and Discharge vs OFF Pin

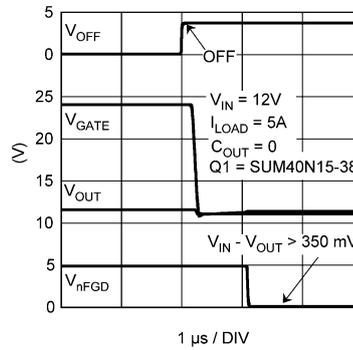


Figure 18. OFF Pin, ON to OFF Transition

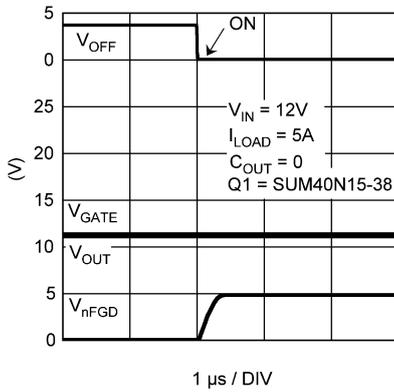


Figure 19. OFF Pin, OFF to ON Transition

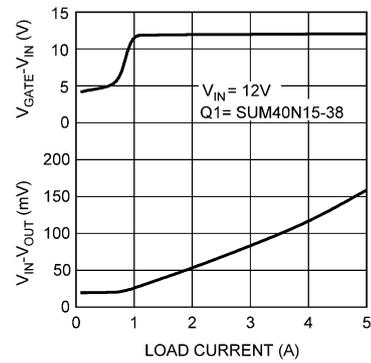


Figure 20. GATE Pin vs  $(R_{DS(ON)} \times I_{DS})$

## Operation Description

### IN, GATE, and OUT Pins

When power is initially applied, the load current will flow from source to drain through the body diode of the MOSFET. Once the voltage across the body diode exceeds  $V_{SD(REG)}$  then the AS5050 begins charging the MOSFET gate through a 32  $\mu\text{A}$  (typical) charge pump current source. In forward operation, the gate of the MOSFET is charged until it reaches the clamping voltage of the 12V GATE to IN pin Zener diode internal to the AS5050.

The AS5050 is designed to regulate the MOSFET gate-to-source voltage. If the MOSFET current decreases to the point that the voltage across the MOSFET falls below the  $V_{SD(REG)}$  voltage regulation point of 22mV (typical), the GATE pin voltage will be decreased until the voltage across the MOSFET is regulated at 22mV. If the source-to-drain voltage is greater than the  $V_{SD(REG)}$  voltage, the gate-to-source voltage will increase and eventually reach the 12V GATE to IN pin Zener clamp level.

If the MOSFET current reverses, possibly due to failure of the input supply, such that the voltage across the AS5050 IN and OUT pins is more negative than the  $V_{SD(REV)}$  voltage of -28mV (typical), the AS5050 will quickly discharge the MOSFET gate through a strong GATE to IN pin discharge transistor.

If the input supply fails abruptly, as would occur if the supply was shorted directly to ground, a reverse current will temporarily flow through the MOSFET until the gate can be fully discharged. This reverse current is sourced from the load capacitance and from the parallel connected supplies. The AS5050 responds to a voltage reversal condition typically within 25ns. The actual time required to turn off the MOSFET will depend on the charge held by the gate capacitance of the MOSFET being used. A MOSFET with 47nF of effective gate capacitance can be turned off in typically 180ns. This fast turnoff time minimizes voltage disturbances at the output, as well as the current transients from the redundant supplies.

### VS Pin

The VS pin of AS5050 is the main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump.

For typical AS5050 applications, where the input voltage is above 5V, the VS pin can be connected directly to the OUT pin. In situations where the input voltage is close to, but not less than, the 5V minimum, it may be helpful to connect the VS pin to the OUT pin through an RC Low-Pass filter to reduce the possibility of erratic behavior due to spurious voltage spikes that may appear on the OUT and IN pins. The series resistor value should be low enough to keep the VS voltage drop at a minimum. A typical series resistor value is 100 $\Omega$ . The capacitor value should be the lowest value that produces acceptable filtering of the voltage noise.

If Vs is powered while IN is floating or grounded, then about 0.5 mA will leak from the Vs pin into the IC and about 3mA will leak from the OUT pin into the IC. From this leakage, about 50 $\mu\text{A}$  will flow out of the IN pin and the rest will flow to ground. This does not affect long term reliability of the IC but may influence circuit design.

Alternately, it is possible to operate the AS5050 with VIN value as low as 1V if the VS pin is powered from a separate supply. This separate VS supply must be from 5V and 75V.

## OFF Pin

The OFF pin is a logic level input pin that is used to control the gate drive to the external MOSFET. The maximum operating voltage on this pin is 5.5V.

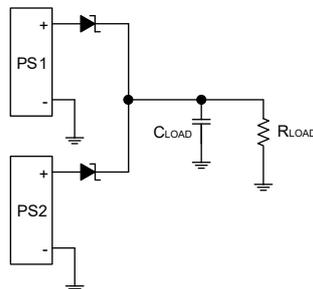
When the OFF pin is high, the MOSFET is turned off (independent of the sensed IN and OUT voltages). In this mode, load current will flow through the body diode of the MOSFET. The voltage difference between the IN pin and OUT pins will be approximately 700mV if the MOSFET is operating normally through the body diode.

The OFF pin has an internal pulldown of 5 $\mu$ A (typical). If the OFF function is not required, the pin may be left open or connected to ground.

## Application and Implementation

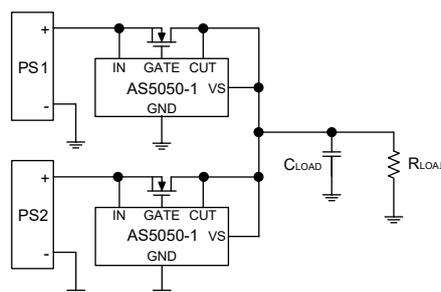
### Application Information

Systems that require high availability often use multiple, parallel-connected redundant power supplies to improve reliability. Schottky OR-ing diodes are typically used to connect these redundant power supplies to a common point at the load. The disadvantage of using OR-ing diodes is the forward voltage drop, which reduces the available voltage and the associated power losses as load currents increase. Using an N-channel MOSFET to replace the OR-ing diode requires a small increase in the level of complexity, but reduces, or eliminates, the need for diode heat sinks or large thermal copper area in circuit board layouts for high power applications.



OR-ing with Diodes

The AS5050 is a positive voltage (that is, high-side) OR-ing controller that will drive an external N-channel MOSFET to replace an OR-ing diode. The voltage across the MOSFET source and drain pins is monitored by the AS5050 at the IN and OUT pins, while the GATE pin drives the MOSFET to control its operation based on the monitored source-drain voltage. The resulting behavior is that of an ideal rectifier with source and drain pins of the MOSFET acting as the anode and cathode pins of a diode respectively.



OR-ing With MOSFETs

## MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous Drain current  $I_D$ , the maximum Source current (that is, body diode)  $I_S$ , the maximum drain-to-source voltage  $V_{DS(MAX)}$ , the gate-to-source threshold voltage  $V_{GS(TH)}$ , the drain-to-source reverse breakdown voltage  $V_{(BR)DSS}$ , and the drain-to-source On resistance  $R_{DS(ON)}$ .

The maximum continuous drain current,  $I_D$ , rating must exceed the maximum continuous load current. The rating for the maximum current through the body diode,  $I_S$ , is typically rated the same as, or slightly higher than the drain current, but body diode current only flows while the MOSFET gate is being charged to  $V_{GS(TH)}$ .

Gate Charge Time =  $Q_g / I_{GATE(ON)}$

1. The maximum drain-to-source voltage,  $V_{DS(MAX)}$ , must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions.
2. The drain-to-source reverse breakdown voltage,  $V_{(BR)DSS}$ , may provide some transient protection to the OUT pin in low voltage applications by allowing conduction back to the IN pin during positive transients at the OUT pin.
3. The gate-to-source threshold voltage,  $V_{GS(TH)}$ , should be compatible with the AS5050 gate drive capabilities. Logic level MOSFETs, with  $R_{DS(ON)}$  rated at  $V_{GS(TH)}$  at 5V, are recommended, but sub-Logic level MOSFETs having  $R_{DS(ON)}$  rated at  $V_{GS(TH)}$  at 2.5V, can also be used.
4. The dominate MOSFET loss for the AS5050 active OR-ing controller is conduction loss due to source-to- drain current to the output load, and the  $R_{DS(ON)}$  of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible  $R_{DS(ON)}$ . However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low  $R_{DS(ON)}$  may not always give desirable results for several reasons:
  1. Reverse transition detection. Higher  $R_{DS(ON)}$  will provide increased voltage information to the AS5050 Reverse Comparator at a lower reverse current level. This will give an earlier MOSFET turnoff condition should the input voltage become shorted to ground. This will minimize any disturbance of the redundant bus.
  2. Reverse current leakage. In cases where multiple input supplies are closely matched it may be possible for some small current to flow continuously through the MOSFET drain to source (that is, reverse) without activating the AS5050 Reverse Comparator. Higher  $R_{DS(ON)}$  will reduce this reverse current level.
  3. Cost. Generally, as the  $R_{DS(ON)}$  rating goes lower, the cost of the MOSFET goes higher.
5. The dominate MOSFET loss for the AS5050 active OR-ing controller is conduction loss due to source-to- drain current to the output load, and the  $R_{DS(ON)}$  of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible  $R_{DS(ON)}$ . However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low  $R_{DS(ON)}$  may not always give desirable results for several reasons:
  - a. Selecting a MOSFET with an  $R_{DS(ON)}$  that is too large will result in excessive power dissipation. Additionally, the MOSFET gate will be charged to the full value that the AS5050 can provide as it attempts to drive the Drain to Source voltage down to the  $V_{SD(REG)}$  of 22mV typical. This increased Gate charge will require some finite amount of additional discharge time when the MOSFET needs to be turned off.

b. As a guideline, it is suggested that  $R_{DS(ON)}$  be selected to provide at least 22mV, and no more than 100mV, at the nominal load current.

c.  $(22mV / I_D) \leq R_{DS(ON)} \leq (100mV / I_D)$

d. The thermal resistance of the MOSFET package should also be considered against the anticipated dissipation in the MOSFET to ensure that the junction temperature ( $T_J$ ) is reasonably well controlled, because the  $R_{DS(ON)}$  of the MOSFET increases as the junction temperature increases.

6.  $P_{DISS} = I_D^2 \times (R_{DS(ON)})$

7. Operating with a maximum ambient temperature ( $T_{A(MAX)}$ ) of 35°C, a load current of 10 A, and an  $R_{DS(ON)}$  of 10mΩ, and desiring to keep the junction temperature under 100°C, the maximum junction-to-ambient thermal resistance rating ( $\theta_{JA}$ ) must be:

a.  $R_{\theta JA} \leq (T_{J(MAX)} - T_{A(MAX)}) / (I_D^2 \times R_{DS(ON)})$

b.  $R_{\theta JA} \leq (100^\circ C - 35^\circ C) / (10A \times 10A \times 0.01\Omega)$

c.  $R_{\theta JA} \leq 65^\circ C/W$

### Short Circuit Failure of an Input Supply

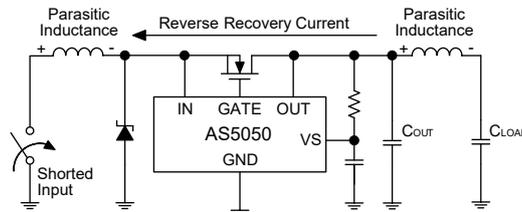
An abrupt 0Ω short circuit across the input supply will cause the highest possible reverse current to flow while the internal AS5050 control circuitry discharges the gate of the MOSFET. During this time, the reverse current is limited only by the  $R_{DS(ON)}$  of the MOSFET, along with parasitic wiring resistances and inductances. Worst case instantaneous reverse current would be limited to:

$$I_{D(REV)} = (V_{OUT} - V_{IN}) / R_{DS(ON)} \quad (1)$$

The internal Reverse Comparator will react, and will start the process of discharging the Gate, when the reverse current reaches:

$$I_{D(REV)} = V_{SD(REV)} / R_{DS(ON)} \quad (2)$$

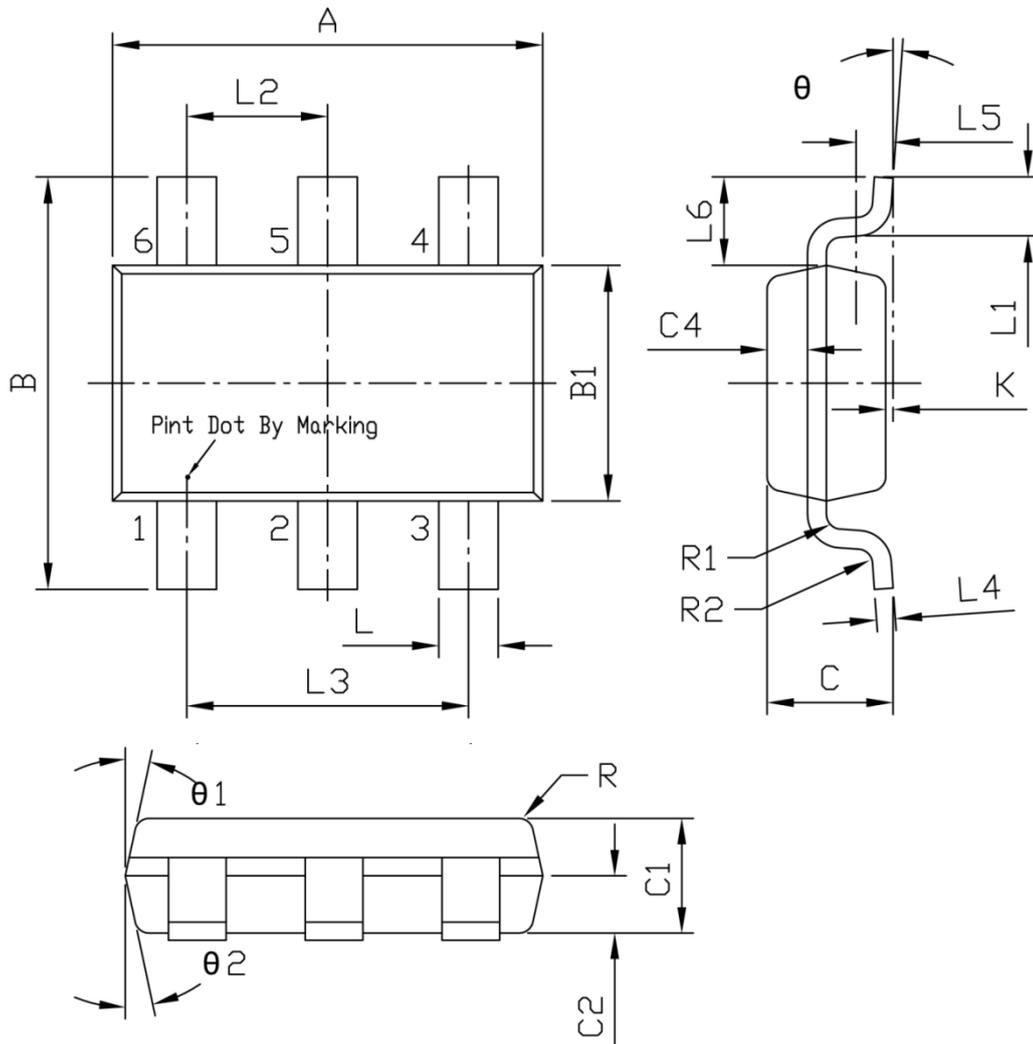
When the MOSFET is finally switched off, the energy stored in the parasitic wiring inductances will be transferred to the rest of the circuit. As a result, the AS5050 IN pin will see a negative voltage spike while the OUT pin will see a positive voltage spike. The IN pin can be protected by diode clamping the pin to GND in the negative direction. The OUT pin can be protected with a TVS protection diode, a local bypass capacitor, or both. In low voltage applications, the MOSFET drain to- source breakdown voltage rating may be adequate to protect the OUT pin (that is,  $V_{IN} + V_{(BR)DSS(MAX)} < 75V$ ), but most MOSFET data sheets do not ensure the maximum breakdown rating, so this method should be used with caution.



Reverse Recovery Current Generates Inductive Spikes at  $V_{IN}$  and  $V_{OUT}$  pins

## Package Information

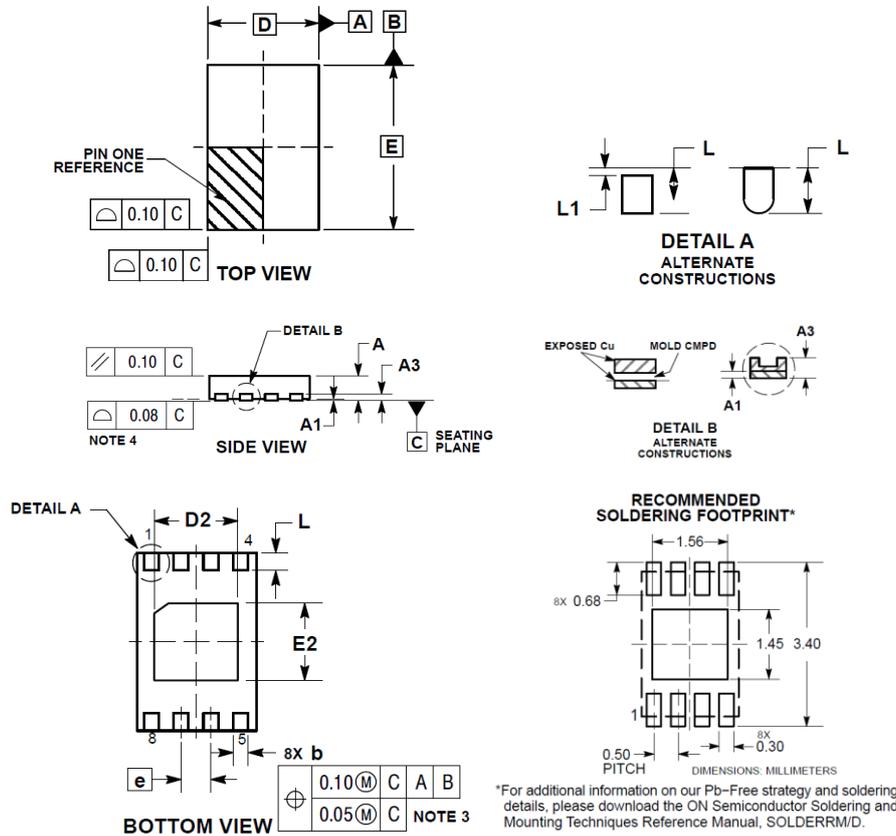
### SOT23-6L



Unit: mm

Symbol	Dimensions In Millimeters			Symbol	Dimensions In Millimeters		
	Min	Typ	Max		Min	Typ	Max
A	2.80	2.90	3.00	L3	1.800	1.900	2.000
B	2.60	2.80	3.00	L4	0.077	0.127	0.177
B1	1.50	1.60	1.70	L5	-	0.250	-
C	-	-	1.05	L6	-	0.600	-
C1	0.60	0.80	1.00	theta	0°		0°
C2	0.35	0.40	0.45	theta1	10°	12°	14°
C4	0.223	0.273	0.323	theta2	10°	12°	14°
K	0.000	0.075	0.150	R	-	0.100	-
L	0.325	0.400	0.475	R1	-	0.100	-
L1	0.325	0.450	0.550	R2	-	0.100	-
L2	0.850	0.950	1.050				

DFN3\*2-8L



NOTES:  
 DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.  
 CONTROLLING DIMENSION: MILLIMETERS.  
 DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN  
 AND 0.25MM FROM THE TERMINAL TIP.  
 COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.45		0.55
A1	0		0.05
A3		0.13	
b	0.2		0.3
D		2	
D2	1.35		1.45
E		3	
E2	1.25		1.35
e		0.5	
L	0.25		0.35
L1			0.15