

100V Input High-Side OR-ing FET Controller

General Description

The AS5051 high-side OR-ing FET controller works with an external MOSFET and acts as an ideal diode rectifier when connected in series with the power supply. This OR-ing controller enables MOSFETs to replace diode rectifiers in power distribution networks, reducing power loss and voltage drop.

The AS5051 controller provides charge pump gate drive for an external N-channel MOSFET and fast response comparator to turn off the FET when current flows in reverse.

The AS5051 can be connected to power supplies from 1V to 100V (a separate VS supply is needed when IN is 1V to 4V) and can withstand transient voltages up to 110V.

Features

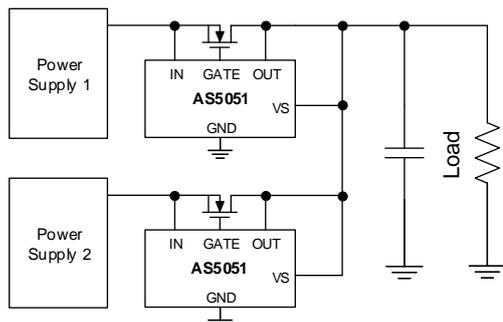
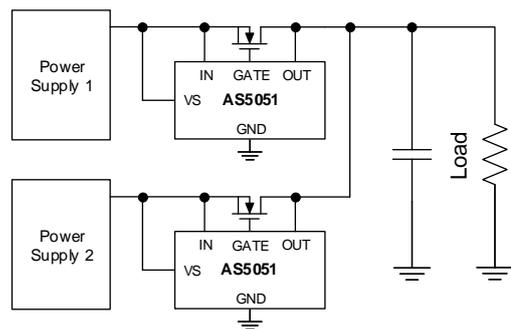
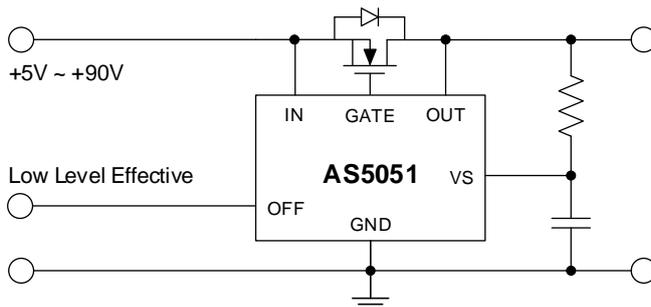
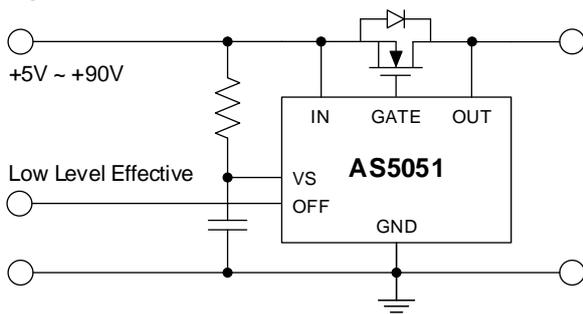
- Wide input voltage range: 5V to 100V
- 110V transient voltage
- Charge pump gate driver for external N-channel MOSFET
- 50ns fast response to current reversal
- 2A peak gate off current
- Ultra-small VDS turn-off voltage reduces turn-off time
- 8-Pin DFN2*3 and SOP-8

Applications

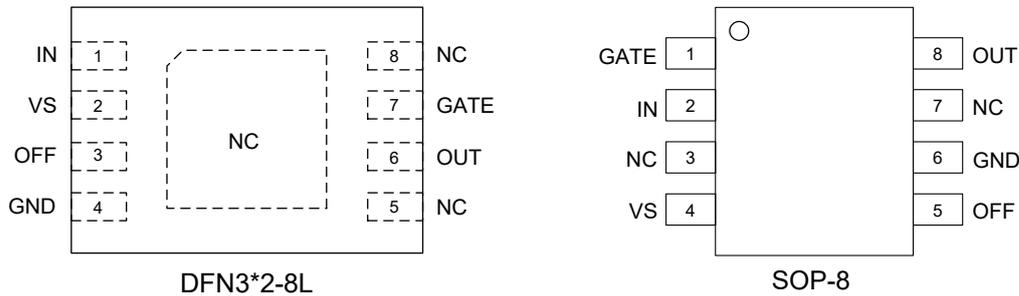
- Active OR-ing of redundant (N+1) power supplies

Typical Application Circuit

VS is connected to VIN is recommended to reduce reverse leakage current during shutdown



Pin Configuration



Pin Descriptions

PIN NO.		PIN name	Description
DFN	SOP		
1	2	IN	Voltage sense connection to the external MOSFET Source pin.
2	4	VS	The main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump. Typically connected to either VOUT or VIN; a separate supply can also be used. VS is connected to VIN is recommended to reduce leakage current during reverse shutdown mode.
3	5	OFF	A logic high state at the OFF pin will pull the GATE pin low and turn off the external MOSFET. Note that when the MOSFET is off, current will still conduct through the FET's body diode. This pin should may be left open or connected to GND if unused.
4	6	GND	Ground return for the controller
5, 8	3, 7	NC	
6	8	OUT	Voltage sense connection to the external MOSFET Drain pin.
7	1	GATE	Connect to the Gate of the external MOSFET. Controls the MOSFET to emulate a low forward- voltage diode.
Thermal pad		Thermal pad	This pad can be connected to GND.

Ordering Information

PART No.	Package	Logo	Tape&Reel
AS5051	DFN2*3-8L	AS5051	3000PCS
AS5051S	SOP-8	AS5051S	3000PCS

Recommended Operating Condition

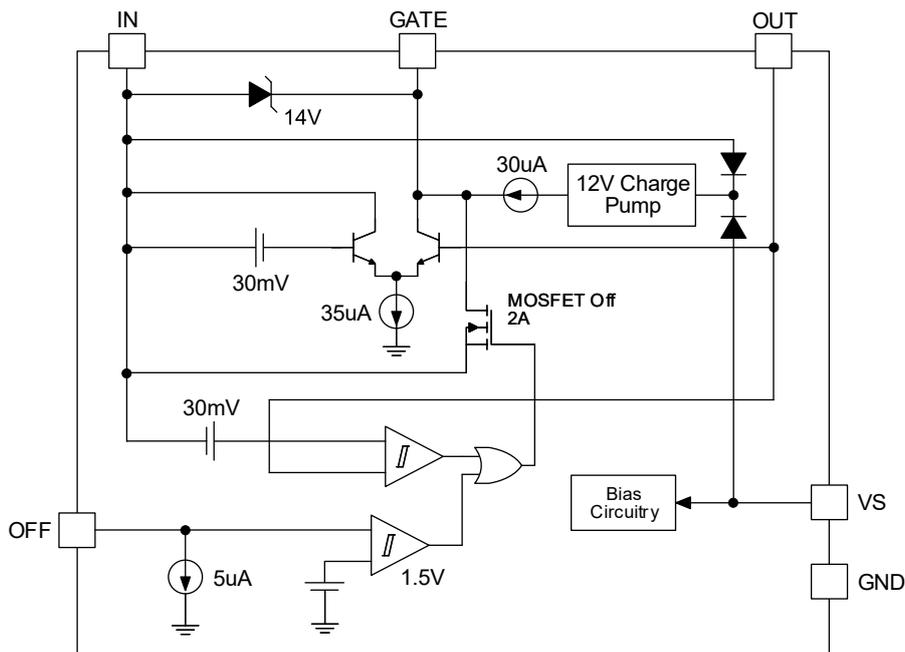
Symbol	Range	Unit
IN, OUT Pins (VS≥4.5V for IN<4V)	1-100	V
VS Pin	5-100	V
OFF Pin	0-5.5	V
Operating temperature	-40~125	°C
Moisture sensitive level	MSL3	

Absolute Maximum Ratings

Parameter	Value	Unit
IN, OUT Pins to GND	-0.3 to 100	V
GATE Pin to GND	-0.3 to 110	V
VS Pin to Ground	-0.3 to 100	V
OFF Pin to Ground	-0.3 to 7	V
Junction temperature	150	°C
Storage temperature, Tstg	-55 to 150	°C
Leading temperature (soldering, 10secs)	260	°C
ESD Susceptibility HBM	±2000	V

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

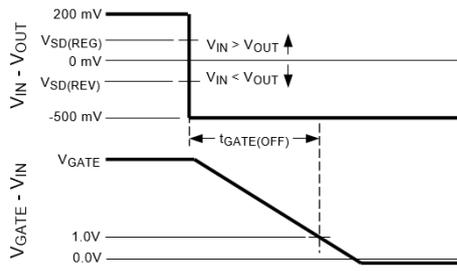
Block Diagram



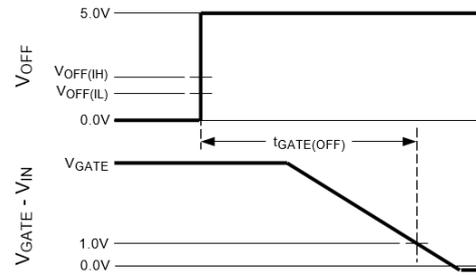
Electrical Characteristics

($V_{IN} = 12V$, $V_{VS} = V_{IN}$, $V_{OUT} = V_{IN}$, $V_{OFF} = 0V$, $C_{GATE} = 47nF$, $T_A = 25^\circ C$, unless otherwise noted)

Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
VS PIN						
V_{VS}	Operating Supply Voltage Range		5		100	V
I_{VS}	Operating Supply Current	$V_{VS} = 5V, V_{IN} = 5V, V_{OUT} = V_{IN} - 100mV$		50	70	uA
		$V_{VS} = 12V, V_{IN} = 5V, V_{OUT} = V_{IN} - 100mV$		55	70	
		$V_{VS} = 40V, V_{IN} = 5V, V_{OUT} = V_{IN} - 100mV$		60	100	
		$V_{VS} = 90V, V_{IN} = 5V, V_{OUT} = V_{IN} - 100mV$		65	110	
IN PIN						
V_{IN}	Operating Input Voltage Range		5		100	V
I_{IN}	IN Pin current	$V_{IN} = 10V, V_{VS} = V_{IN}, V_{OUT} = V_{IN} - 100mV, GATE = Open$	200		500	uA
		$V_{IN} = 12V \text{ to } 90V, V_{VS} = V_{IN}, V_{OUT} = V_{IN} - 100mV, GATE = Open$	250		550	
OUT PIN						
V_{OUT}	Operating Output Voltage Range		5		100	V
I_{OUT}	OUT Pin Current	$V_{IN} = 5V \text{ to } 100V, V_{VS} = V_{IN}, V_{OUT} = V_{IN} - 100mV$		3.2	8	uA
GATE PIN						
$I_{GATE(ON)}$	Gate Pin Source Current	$V_{IN} = 5V, V_{VS} = V_{IN}, V_{GATE} = V_{IN}, V_{OUT} = V_{IN} - 175mV$	-37		-25	uA
		$V_{IN} = 12V \text{ to } 100V, V_{VS} = V_{IN}, V_{GATE} = V_{IN}, V_{OUT} = V_{IN} - 175mV$	-39		-25	
V_{GS}	$V_{GATE} - V_{IN}$ in Forward Operation	$V_{IN} = 5V, V_{VS} = V_{IN}, V_{OUT} = V_{IN} - 175mV$	5	7	8	V
		$V_{IN} = 8V \text{ to } 100V, V_{VS} = V_{IN}, V_{OUT} = V_{IN} - 175mV$	8	11	14	
$t_{GATE(REV)}$	Gate Capacitance Discharge Time at Forward to Reverse Transition	$C_{GATE} = 0$		300		ns
		$C_{GATE} = 10nF$		400		
		$C_{GATE} = 47nF$		500		
$t_{GATE(OFF)}$	Gate Capacitance Discharge Time at OFF pin Low to High Transition	$C_{GATE} = 47nF$		4.2		us
$I_{GATE(OFF)}$	Gate Pin Sink Current	$V_{GATE} = V_{IN} + 3V, V_{OUT} > V_{IN} + 100mV, t \leq 10ms$		2		A
$V_{SD(REV)}$	Reverse V_{SD} Threshold $V_{IN} < V_{OUT}$	$V_{IN} - V_{OUT}$	-40	-15	-10	mV
$\Delta V_{SD(REV)}$	Reverse V_{SD} Hysteresis			10		mV
$V_{SD(REG)}$	Regulated Forward V_{SD} Threshold $V_{IN} > V_{OUT}$	$V_{IN} = 5V, V_{VS} = V_{IN}, V_{IN} - V_{OUT}$	1	15	30	mV
		$V_{IN} = 12V, V_{VS} = V_{IN}, V_{IN} - V_{OUT}$	5	25	60	
OFF PIN						
$V_{OFF(IH)}$	OFF Input High Threshold Voltage	$V_{OUT} = V_{IN} - 500mV, V_{OFF}$ Rising		1.55	1.8	V
$V_{OFF(IL)}$	OFF Input Low Threshold Voltage	$V_{OUT} = V_{IN} - 500mV, V_{OFF}$ Falling	1.3	1.45		
ΔV_{OFF}	OFF Threshold Voltage Hysteresis	$V_{OFF(IH)} - V_{OFF(IL)}$		150		mV
I_{OFF}	OFF Pin Internal Pulldown	$V_{OFF} = 5V$	3	5	8	uA



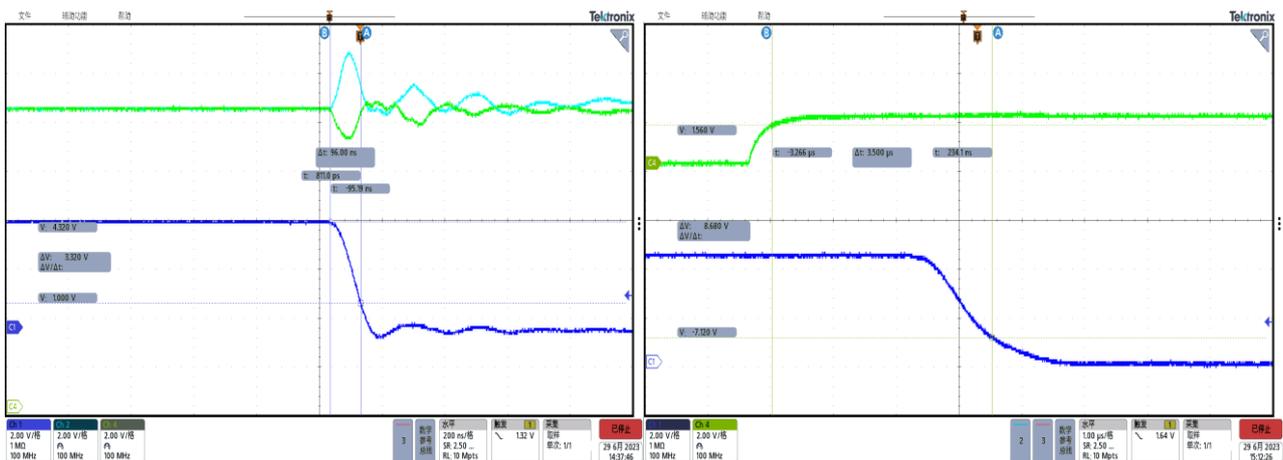
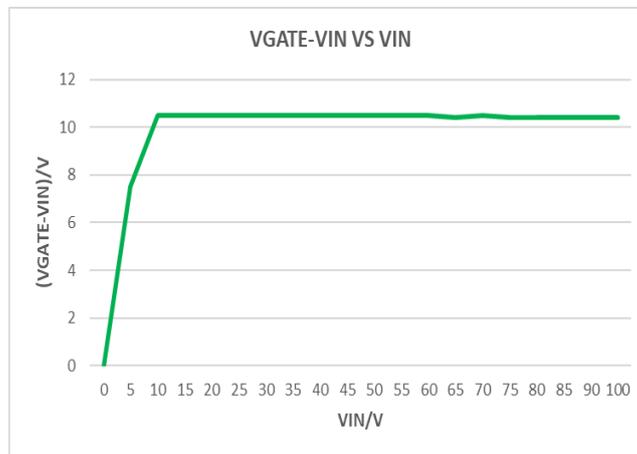
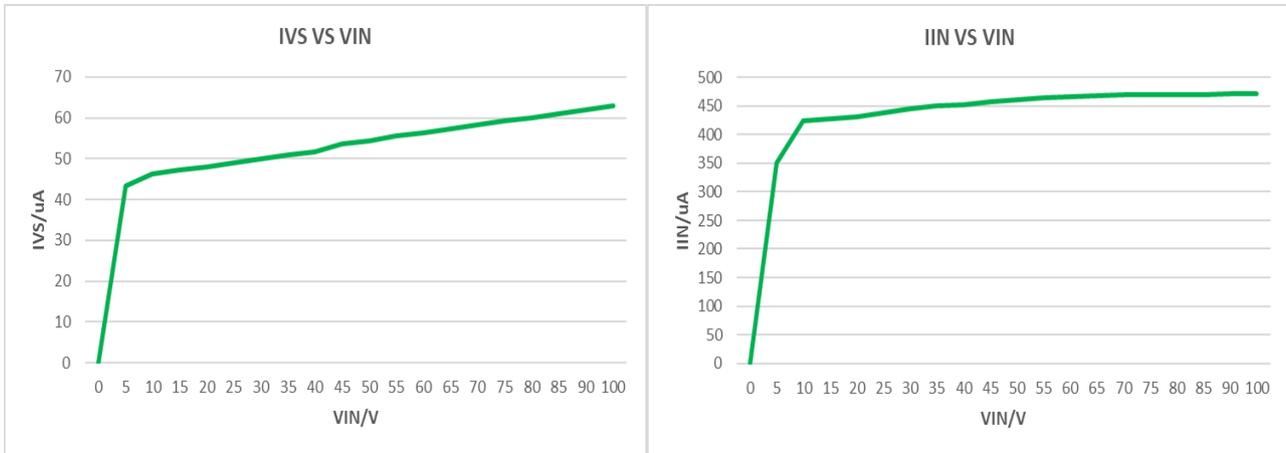
Gate OFF Timing for Forward to Reverse Transition



Gate OFF Timing for OFF Pin Low to High Transition

Characteristic Plots

($V_{IN} = V_{VS} = V_{OUT}$, $V_{OFF} = 0V$, $C_{GATE} = 47nF$, $T_A = 25^\circ C$, unless otherwise noted)



Reverse C_{GATE} discharge time

C_{GATE} discharge time VS OFF pin

Operation Description

IN, GATE, and OUT Pins

When power is initially applied, the load current will flow from source to drain through the body diode of the MOSFET. Once the voltage across the body diode exceeds $V_{SD(REG)}$ then the AS5051 begins charging the MOSFET gate through a 30 μ A (typical) charge pump current source. In forward operation, the gate of the MOSFET is charged until it reaches the clamping voltage of the 14V GATE to IN pin Zener diode internal to the AS5051.

The AS5051 is designed to regulate the MOSFET gate-to-source voltage. If the MOSFET current decreases to the point that the voltage across the MOSFET falls below the $V_{SD(REG)}$ voltage regulation point of 30mV (typical), the GATE pin voltage will be decreased until the voltage across the MOSFET is regulated at 20mV. If the source-to-drain voltage is greater than the $V_{SD(REG)}$ voltage, the gate-to-source voltage will increase and eventually reach the 14V GATE to IN pin Zener clamp level.

If the MOSFET current reverses, possibly due to failure of the input supply, such that the voltage across the AS5051 IN and OUT pins is more negative than the $V_{SD(REV)}$ voltage of -15mV (typical), the AS5051 will quickly discharge the MOSFET gate through a strong GATE to IN pin discharge transistor. If the input supply fails abruptly, as would occur if the supply was shorted directly to ground, a reverse current will temporarily flow through the MOSFET until the gate can be fully discharged. This reverse current is sourced from the load capacitance and from the parallel connected supplies. The AS5051 responds to a voltage reversal condition typically within 50ns. The actual time required to turn off the MOSFET will depend on the charge held by the gate capacitance of the MOSFET being used. A MOSFET with 47nF of effective gate capacitance can be turned off in typically 260ns. This fast turnoff time minimizes voltage disturbances at the output, as well as the current transients from the redundant supplies.

VS Pin

The VS pin of AS5051 is the main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump.

For typical AS5051 applications, the VS pin can be connected directly to the OUT pin. The capacitor value should be the lowest value that produces acceptable filtering of the voltage noise.

If VS is powered while IN is floating or grounded, then about 0.5mA will leak from the VS pin into the IC and about 2mA will leak from the OUT pin into the IC.

OFF Pin

The OFF pin is a logic level input pin that is used to control the gate drive to the external MOSFET. The maximum operating voltage on this pin is 5.5V.

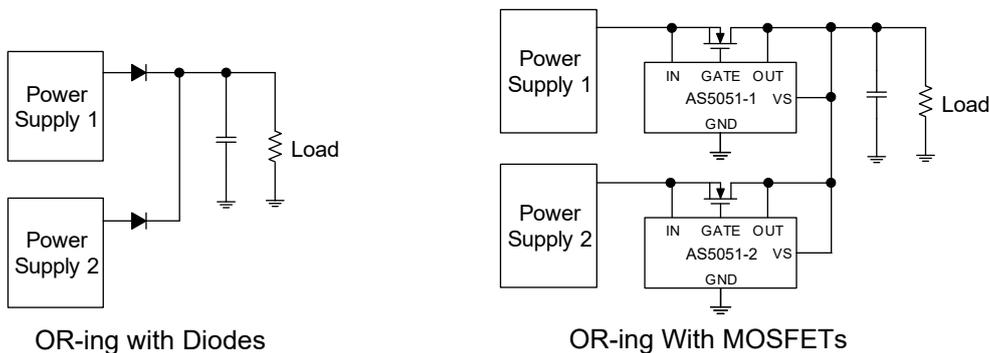
When the OFF pin is high, the MOSFET is turned off (independent of the sensed IN and OUT voltages). In this mode, load current will flow through the body diode of the MOSFET. The voltage difference between the IN pin and OUT pins will be approximately 700mV if the MOSFET is operating normally through the body diode.

The OFF pin has an internal pulldown of 5 μ A (typical). If the OFF function is not required, the pin may be left open or connected to ground.

Application and Implementation

Application Information

Systems that require high availability often use multiple, parallel-connected redundant power supplies to improve reliability. Schottky OR-ing diodes are typically used to connect these redundant power supplies to a common point at the load. The disadvantage of using OR-ing diodes is the forward voltage drop, which reduces the available voltage and the associated power losses as load currents increase. Using an N-channel MOSFET to replace the OR-ing diode requires a small increase in the level of complexity, but reduces, or eliminates, the need for diode heat sinks or large thermal copper area in circuit board layouts for high power applications.



The AS5051 is a positive voltage (that is, high-side) OR-ing controller that will drive an external N-channel MOSFET to replace an OR-ing diode. The voltage across the MOSFET source and drain pins is monitored by the AS5051 at the IN and OUT pins, while the GATE pin drives the MOSFET to control its operation based on the monitored source-drain voltage. The resulting behavior is that of an ideal rectifier with source and drain pins of the MOSFET acting as the anode and cathode pins of a diode respectively.

MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous Drain current I_D , the maximum Source current (that is, body diode) I_S , the maximum drain-to-source voltage $V_{DS(MAX)}$, the gate-to-source threshold voltage $V_{GS(TH)}$, the drain-to-source reverse breakdown voltage $V_{(BR)DSS}$, and the drain-to-source on resistance $R_{DS(ON)}$.

The maximum continuous drain current, I_D , rating must exceed the maximum continuous load current. The rating for the maximum current through the body diode, I_S , is typically rated the same as, or slightly higher than the drain current, but body diode current only flows while the MOSFET gate is being charged to $V_{GS(TH)}$.

$$\text{Gate Charge Time} = Q_g / I_{GATE(ON)}$$

1. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions.
2. The drain-to-source reverse breakdown voltage, $V_{(BR)DSS}$, may provide some transient protection to the OUT pin in low voltage applications by allowing conduction back to the IN pin during positive transients at the OUT pin.
3. The gate-to-source threshold voltage, $V_{GS(TH)}$, should be compatible with the AS5051 gate drive capabilities. Logic level MOSFETs, with $R_{DS(ON)}$ rated at $V_{GS(TH)}$ at 5V, are recommended, but sub-Logic level MOSFETs having $R_{DS(ON)}$ rated at $V_{GS(TH)}$ at 2.5V, can also be used.

4. The dominate MOSFET loss for the AS5051 active OR-ing controller is conduction loss due to source-to- drain current to the output load, and the $R_{DS(ON)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(ON)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(ON)}$ may not always give desirable results for several reasons:

a. Reverse transition detection. Higher $R_{DS(ON)}$ will provide increased voltage information to the AS5051 Reverse Comparator at a lower reverse current level. This will give an earlier MOSFET turnoff condition should the input voltage become shorted to ground. This will minimize any disturbance of the redundant bus.

b. Reverse current leakage. In cases where multiple input supplies are closely matched it may be possible for some small current to flow continuously through the MOSFET drain to source (that is, reverse) without activating the AS5051 Reverse Comparator. Higher $R_{DS(ON)}$ will reduce this reverse current level.

c. Cost. Generally, as the $R_{DS(ON)}$ rating goes lower, the cost of the MOSFET goes higher.

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a. Selecting a MOSFET with an $R_{DS(ON)}$ that is too large will result in excessive power dissipation. Additionally, the MOSFET gate will be charged to the full value that the AS5051 can provide as it attempts to drive the Drain to Source voltage down to the $V_{SD(REG)}$ of 30mV typical. This increased Gate charge will require some finite amount of additional discharge time when the MOSFET needs to be turned off.

b. As a guideline, it is suggested that $R_{DS(ON)}$ be selected to provide at least 30mV, and no more than 100mV, at the nominal load current.

c. $(30mV / I_D) \leq R_{DS(ON)} \leq (100mV / I_D)$

d. The thermal resistance of the MOSFET package should also be considered against the anticipated dissipation in the MOSFET to ensure that the junction temperature (T_J) is reasonably well controlled, because the $R_{DS(ON)}$ of the MOSFET increases as the junction temperature increases.

6. $P_{DISS} = I_D^2 \times (R_{DS(ON)})$

7. Operating with a maximum ambient temperature ($T_{A(MAX)}$) of 35°C, a load current of 10A, and an $R_{DS(ON)}$ of 10mΩ, and desiring to keep the junction temperature under 100°C, the maximum junction-to-ambient thermal resistance rating (θ_{JA}) must be:

a. $R_{\theta JA} \leq (T_{J(MAX)} - T_{A(MAX)}) / (I_D^2 \times R_{DS(ON)})$

b. $R_{\theta JA} \leq (100^\circ C - 35^\circ C) / (10A \times 10A \times 0.01\Omega)$

c. $R_{\theta JA} \leq 65^\circ C/W$

Short Circuit Failure of an Input Supply

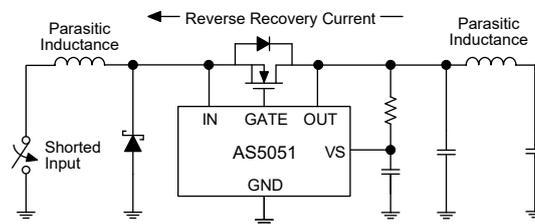
An abrupt 0Ω short circuit across the input supply will cause the highest possible reverse current to flow while the internal AS5051 control circuitry discharges the gate of the MOSFET. During this time, the reverse current is limited only by the $R_{DS(ON)}$ of the MOSFET, along with parasitic wiring resistances and inductances. Worst case instantaneous reverse current would be limited to:

$$I_{D(REV)} = (V_{OUT} - V_{IN}) / R_{DS(ON)} \quad (1)$$

The internal Reverse Comparator will react, and will start the process of discharging the Gate, when the reverse current reaches:

$$I_{D(REV)} = V_{SD(REV)} / R_{DS(ON)} \quad (2)$$

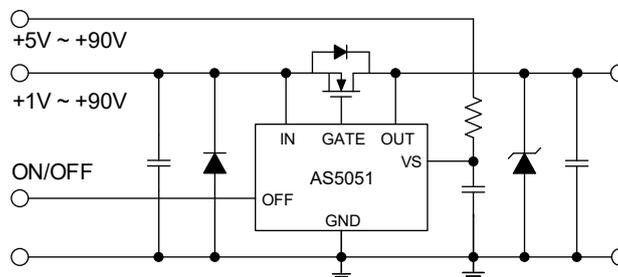
When the MOSFET is finally switched off, the energy stored in the parasitic wiring inductances will be transferred to the rest of the circuit. As a result, the AS5051 IN pin will see a negative voltage spike while the OUT pin will see a positive voltage spike. The IN pin can be protected by diode clamping the pin to GND in the negative direction. The OUT pin can be protected with a TVS protection diode, a local bypass capacitor, or both. In low voltage applications, the MOSFET drain to- source breakdown voltage rating may be adequate to protect the OUT pin (that is, $V_{IN} + V_{(BR)DSS(MAX)} < 40V$), but most MOSFET data sheets do not ensure the maximum breakdown rating, so this method should be used with caution.



Reverse Recovery Current Generates Spikes at V_{IN} and V_{OUT}

A Separate VS Supply for Low Vin Operation

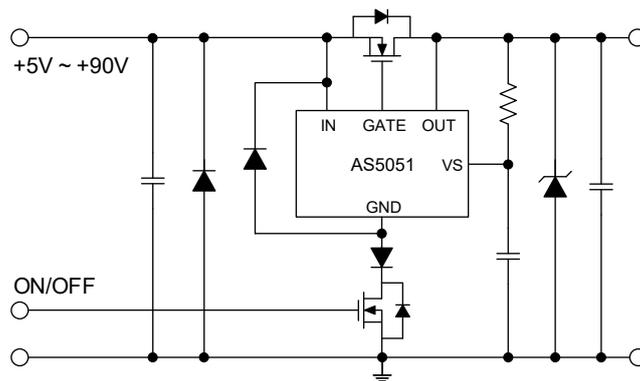
In some applications, it is desired to operate AS5051 from low supply voltage. The AS5051 can operate with a 1V rail voltage, provides its VS pin is biased from 5V to 40. The detail of such application is depicted in the next figure.



Reverse Input Voltage Protection with IQ Reduction

If VS is powered while IN is floating or grounded, then about 0.5mA will leak from the VS pin into the IC and about 3mA will leak from the OUT pin into the IC. From this leakage, about 0.05mA will flow out of the IN pin and the rest will flow to ground. This does not affect long term reliability of the IC, but may influence circuit design.

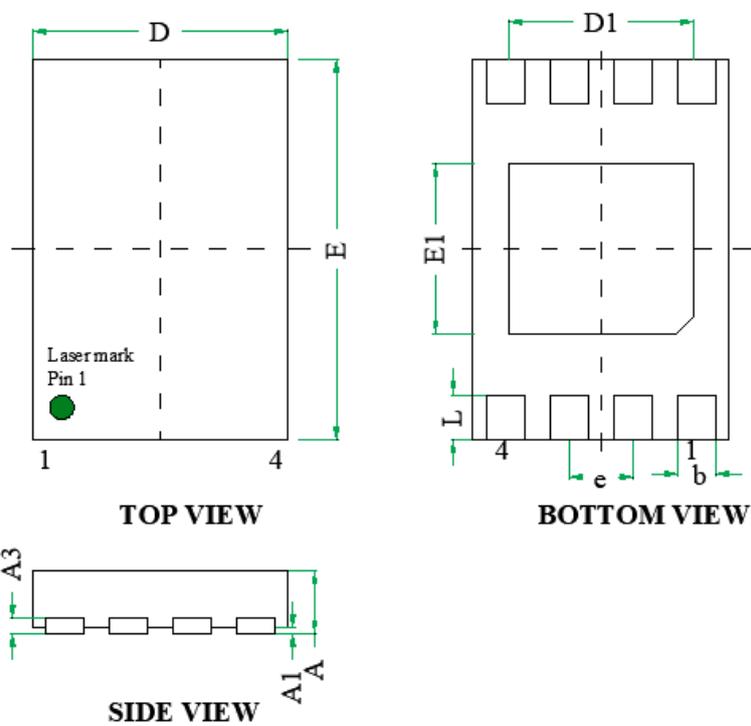
In battery powered applications, whenever AS5051 functionality is not needed, the supply to the AS5051 can be disconnected by turning OFF Q2, as shown in the following figure. This disconnects to the ground path of the AS5051 and eliminates the current leakage from the battery.



Reverse input voltage protection with IQ reduction schematic

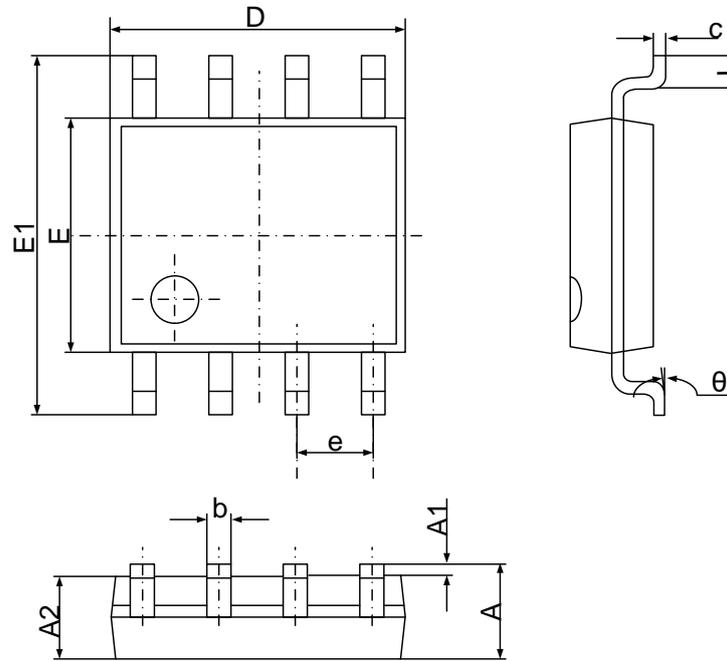
Package Information

DFN2*3-8L



SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.5	0.55	0.6
A1	0	0.025	0.05
A3		0.152BSC	
D	1.95	2	2.05
E	2.95	3	3.05
D1	1.5	1.65	1.75
E1	1.65	1.8	1.9
b	0.2	0.25	0.3
e		0.500BSC	
L	0.3	0.4	0.5

SOP-8



符号	尺寸 (毫米)		尺寸 (英寸)	
	最小	最大	最小	最大
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (中心到中心)		0.050 (中心到中心)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°