High-Side OR-ing FET Controller

General Description

The AS5052 high-side OR-ing works with an internal MOSFET and acts as an ideal diode rectifier when connected in series with the power supply. This OR-ing circuit enables MOSFETs to replace diode rectifiers in power distribution networks, reducing power loss and voltage drop. The AS5052 controller provides charge pump gate drive for an internal N-channel MOSFET and fast response comparator to turn off the FET when current flows in reverse. The AS5052 can be connected to power supplies from 1V to 40V (a separate VS supply is needed when IN is 1V to 4V) and can withstand transient voltages up to 60V.

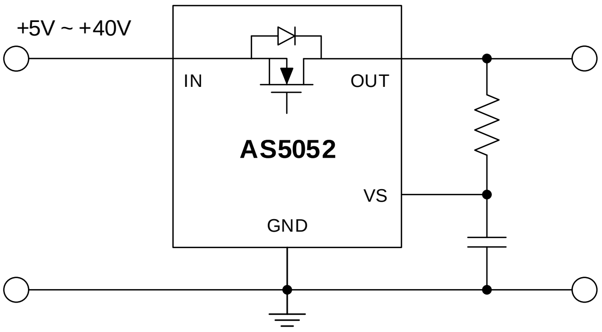
Features

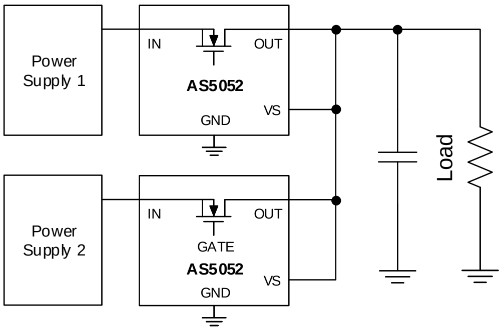
- Wide operating input voltage range V_{IN}: 5V to 40V
- 60V transient voltage
- Charge pump gate driver for internal N-channel MOSFET
- 50ns fast response to current reversal
- 2A peak gate off current internal
- Ultra-small V_{DS} turn-off voltage reduces turn-off time
- 8-Pin SOP8L

Applications

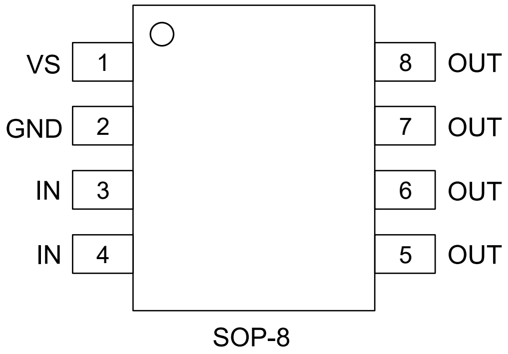
- Active OR-ing of redundant (N+1) power supplies

Typical Application Circuit





Pin Configuration



Pin Descriptions

PIN NO.	PIN name	Description
1	VS	The main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump. Typically connected to either V_{OUT} or V_{IN}; a separate supply can also be used.
2	GND	Ground return for the controller
3, 4	IN	Voltage sense connection to the external MOSFET source pin.
5~8	OUT	Voltage sense connection to the external MOSFET drain pin.

Ordering Information

PART No.	Package	Logo	Tape&Reel
AS5052	SOP-8	AS5052	3000PCS

Absolute Maximum Ratings

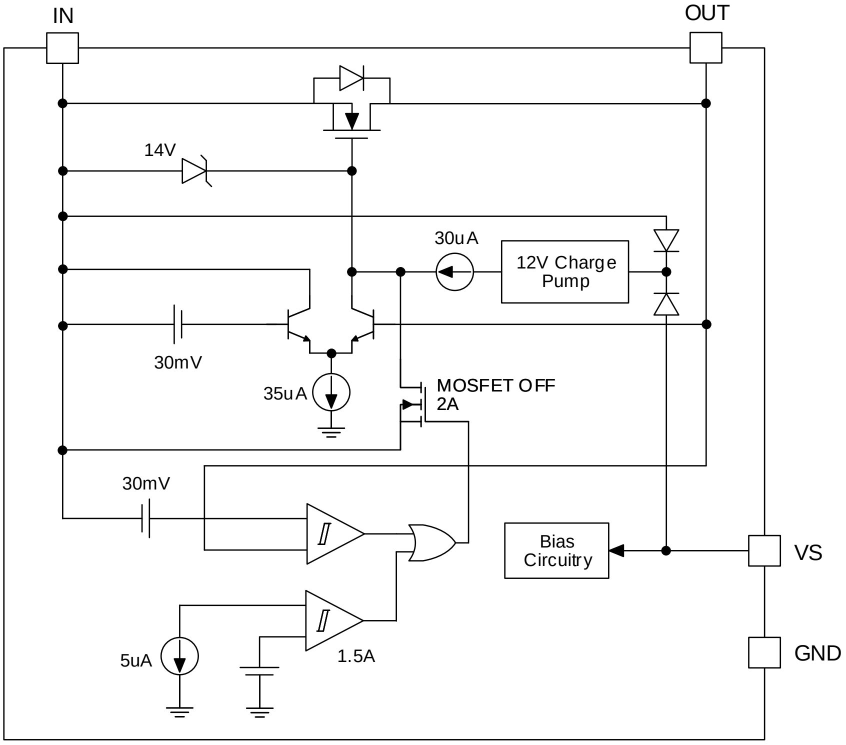
Parameter	Value	Unit
IN, OUT Pins to GND	-0.3 to 50	V
VS Pin to Ground	-0.3 to 50	V
Internal MOSFET VDS	≥60	V
Junction temperature	150	°C
Storage temperature, Tstg	-50 to 150	°C
Leading temperature (soldering, 10secs)	260	°C
ESD Susceptibility HBM	±2000	V

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

Recommended Operating Condition

Symbol	Range	Unit
IN, OUT Pins (VS ≥ 4.5V for IN < 4V)	1-40	V
VS Pin	5-40	V
Operating temperature	-40~125	°C

Block Diagram



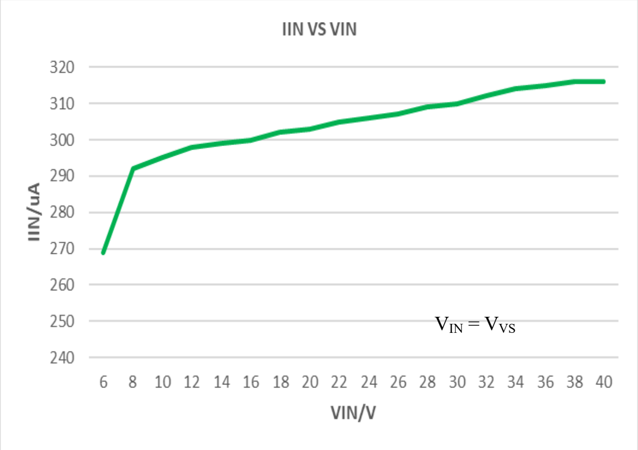
Electrical Characteristics

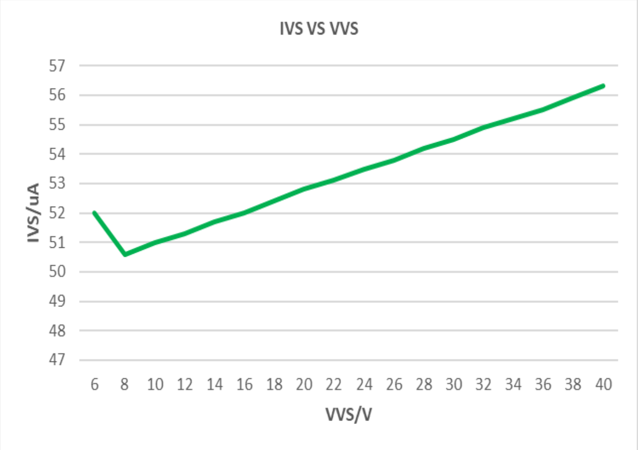
(V_{IN} =12V, V_{VS} = V_{IN}, TA = 25°C, unless otherwise noted)

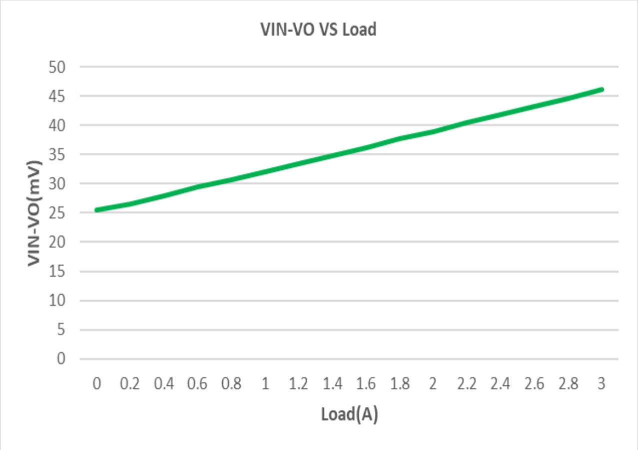
Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
VS PIN						
V_{VS}	Operating Supply Voltage Range		5		40	V
I_{VS}	Operating Supply Current	V_{VS} = 5V, V_{IN} = V_{VS}		50	70	uA
		V_{VS} = 12V, V_{IN} = 5V		52	70	
		V_{VS} = 40V, V_{IN} = 5V		56	100	
IN PIN						
V_{IN}	Operating Input Voltage Range		5		40	V
I_{IN}	IN Pin current	V_{IN} =5V, V_{VS} = V_{IN}	150	240	300	uA
		V_{IN} = 12V to 40V, V_{VS} = V_{IN}	200	300	400	
OUT PIN						
V_{OUT}	Operating Output Voltage Range		5		40	V
I_{OUT}	OUT Pin Current	V_{IN} = 5V to 40V, V_{VS} = V_{IN}		4.1		uA
INTERNAL REGULATOR						
$I_{GATE(OFF)}$	Internal Sink Current	V_{GATE} = V_{IN} + 3V, V_{OUT} > V_{IN} + 100mV, t ≤ 10ms		2		A
$V_{SD(REV)}$	Reverse V_{SD} Threshold $V_{IN} < V_{OUT}$	V_{IN} - V_{OUT}	-40	–28	-20	mV
$V_{SD(REG)}$	Regulated Forward V_{SD} Threshold $V_{IN} > V_{OUT}$	V_{IN} = 5V, V_{VS} = V_{IN}, V_{IN} - V_{OUT}	1	30	40	mV
		V_{IN} = 12V, V_{VS} = V_{IN}, V_{IN} - V_{OUT}	5	60	80	
INTERNAL MOSFET						
V_{DS}	Drain to source voltage	I_{DS} = 250uA	60			V
R_{ON}	On resistance	I_D = 1A		8	12	mΩ

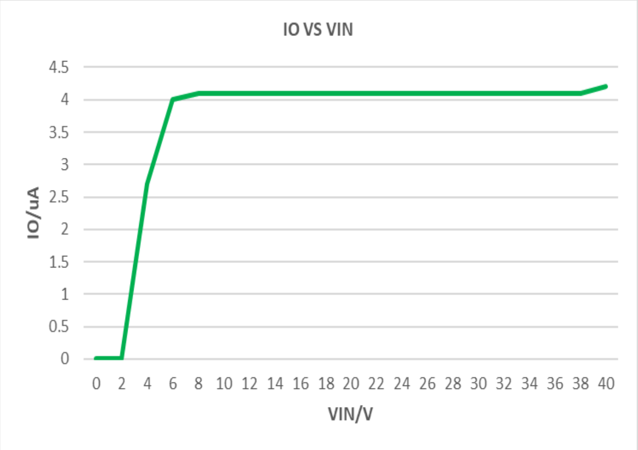
Characteristic Plots

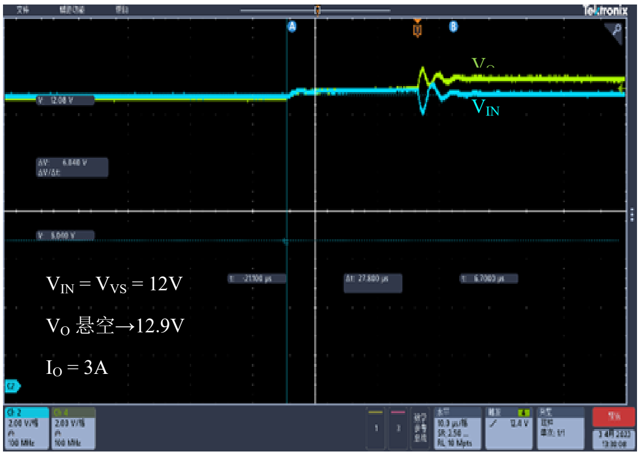
(V_{IN} = V_{VS} = V_{OUT}, T_A = 25°C, unless otherwise noted)

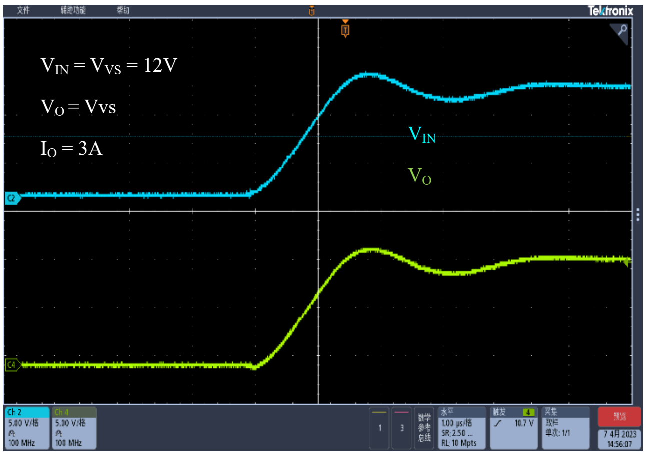












Operation Description

IN and OUT Pins

When power is initially applied, the load current will flow from source to drain through the body diode of the MOSFET. Once the voltage across the body diode exceeds $V_{SD(REG)}$ then the AS5052 begins charging the internal MOSFET gate through a 30μA (typical) charge pump current source. In forward operation, the gate of the internal MOSFET is charged. The AS5052 is designed to regulate the internal MOSFET gate-to-source voltage. If the MOSFET current decreases to the point that the voltage across the MOSFET falls below the $V_{SD(REG)}$ voltage regulation point of 30mV (typical), the internal MOSFET gate voltage will be decreased until the voltage across the MOSFET is regulated at 30mV. If the source-to-drain voltage is greater than the $V_{SD(REG)}$ voltage, the gate-to-source voltage will increase and eventually reach the 12V gate to IN pin Zener clamp level.

If the MOSFET current reverses, possibly due to failure of the input supply, such that the voltage across the AS5052 IN and OUT pins is more negative than the $V_{SD(REV)}$ voltage of -28mV (typical), the AS5052 will quickly discharge the internal MOSFET gate through a strong gate to IN pin discharge transistor. If the input supply fails abruptly, as would occur if the supply was shorted directly to ground, a reverse current will temporarily flow through the MOSFET until the gate can be fully discharged. This reverse current is sourced from the load capacitance and from the parallel connected supplies. The AS5052 responds to a voltage reversal condition typically within 50ns. The actual time required to turn off the MOSFET will depend on the charge held by the gate capacitance of the MOSFET being used. For AS5052, the gate capacitance of the internal MOSFET is 4.6nF and the typical turn off time is 25ns. This fast turnoff time minimizes voltage disturbances at the output, as well as the current transients from the redundant supplies.

VS Pin

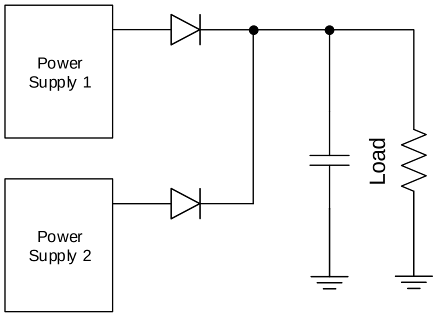
The VS pin of AS5052 is the main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump.

For typical AS5052 applications, the VS pin can be connected directly to the OUT pin. The capacitor value should be the lowest value that produces acceptable filtering of the voltage noise.

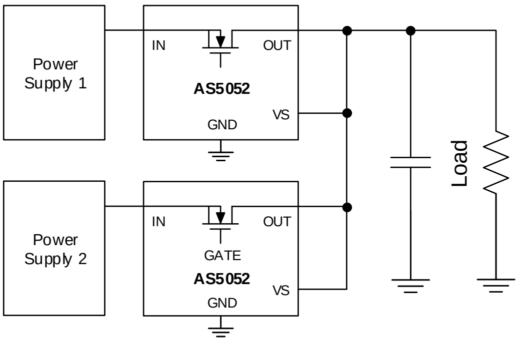
Application and Implementation

Application Information

Systems that require high availability often use multiple, parallel-connected redundant power supplies to improve reliability. Schottky OR-ing diodes are typically used to connect these redundant power supplies to a common point at the load. The disadvantage of using OR-ing diodes is the forward voltage drop, which reduces the available voltage and the associated power losses as load currents increase. Using an N-channel MOSFET to replace the OR-ing diode requires a small increase in the level of complexity, but reduces, or eliminates, the need for diode heat sinks or large thermal copper area in circuit board layouts for high power applications.



OR-ing with Diodes



OR-ing with internal MOSFETs

The AS5052 is a positive voltage (that is, high-side) OR-ing controller that will drive an external N-channel MOSFET to replace an OR-ing diode. The voltage across the MOSFET source and drain pins is monitored by the AS5052 at the IN and OUT pins, while the internal MOSFET gate drives the MOSFET to control its operation based on the monitored source-drain voltage. The resulting behavior is that of an ideal rectifier with source and drain pins of the MOSFET acting as the anode and cathode pins of a diode respectively.

Short Circuit Failure of an Input Supply

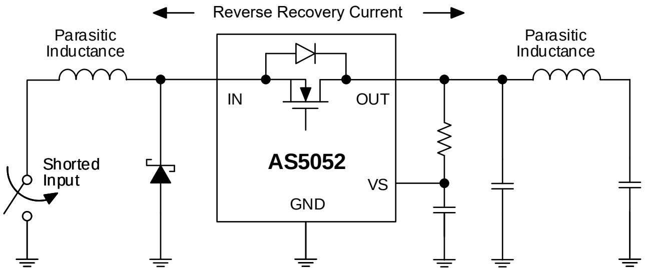
An abrupt 0Ω short circuit across the input supply will cause the highest possible reverse current to flow while the internal AS5052 control circuitry discharges the gate of the MOSFET. During this time, the reverse current is limited only by the $R_{DS(ON)}$ of the MOSFET, along with parasitic wiring resistances and inductances. Worst case instantaneous reverse current would be limited to:

$I_{D(REV)} = (V_{OUT} - V_{IN}) / R_{DS(ON)}$ (1)

The internal Reverse Comparator will react, and will start the process of discharging the internal MOSFET gate, when the reverse current reaches:

$I_{D(REV)} = V_{SD(REV)} / R_{DS(ON)}$ (2)

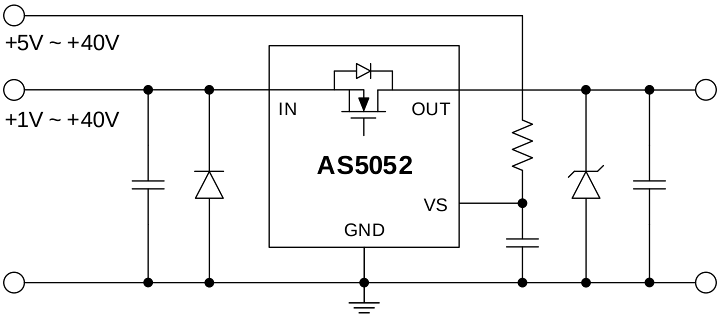
When the MOSFET is finally switched off, the energy stored in the parasitic wiring inductances will be transferred to the rest of the circuit. As a result, the AS5052 IN pin will see a negative voltage spike while the OUT pin will see a positive voltage spike. The IN pin can be protected by diode clamping the pin to GND in the negative direction. The OUT pin can be protected with a TVS protection diode, a local bypass capacitor, or both.



Reverse Recovery Current Generates Spikes at V_{IN} and V_{OUT}

A Separate VS Supply for Low V_{IN} Operation

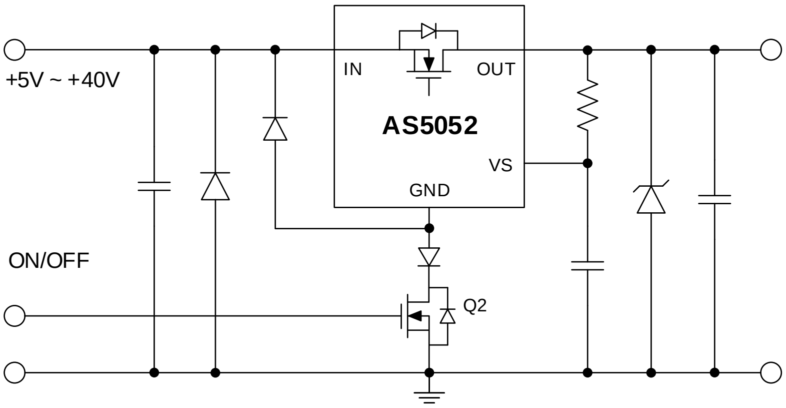
In some applications, it is desired to operate AS5052 from low supply voltage. The AS5052 can operate with a 1V rail voltage, provides its VS pin is biased from 5V to 40V. The detail of such application is depicted in the following figure.



Reverse Input Voltage Protection with IQ Reduction

If VS is powered while IN is floating or grounded, then about 0.5mA will leak from the VS pin into the IC and about 3mA will leak from the OUT pin into the IC. From this leakage, about 0.05mA will flow out of the IN pin and the rest will flow to ground. This does not affect long term reliability of the IC but may influence circuit design.

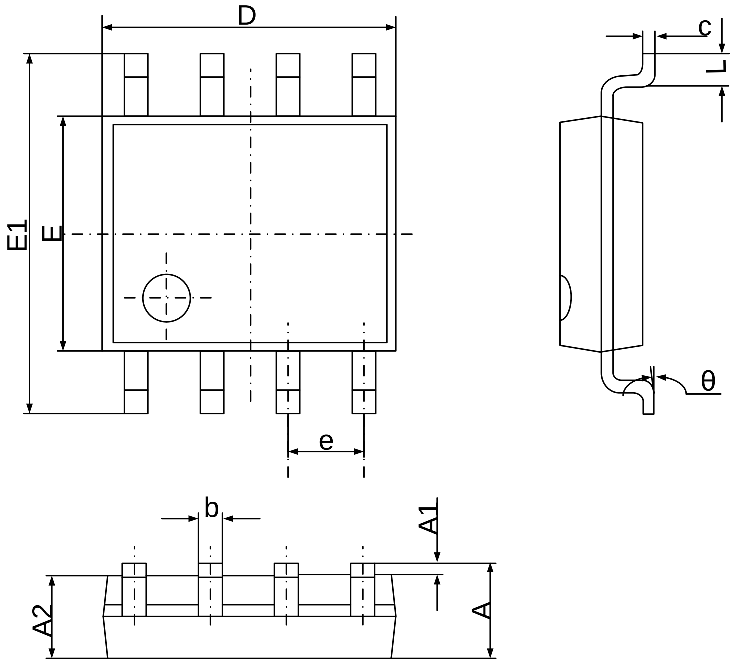
In battery powered applications, whenever AS5052 functionality is not needed, the supply to the AS5052 can be disconnected by turning off Q2, as shown in the following figure. This disconnects to the ground path of the AS5052 and eliminates the current leakage from the battery.



Reverse input voltage protection with IQ reduction schematic

Package Information

SOP-8



符号	尺寸 (毫米)		尺寸 (英寸)	
	最小	最大	最小	最大
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (中心到中心)		0.050 (中心到中心)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°